ROCKLAND

OPERATING MANUAL

MODEL 5100

FREQUENCY SYNTHESIZER

ROCKLAND SYSTEMS CORPORATION

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ROCKLAND SYSTEMS CORPORATION
WEST NYACK, NEW YORK 10994

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CERTIFICATE OF COMPLIANCE

Rockland Systems Corporation certifies that this instrument was thoroughly tested prior to shipment and found to meet or exceed its published specifications.

WARRANTY

Our instruments are warranted against defects in materials and workmanship for one year from the date of shipment.

We will repair or replace products which prove to be defective during the warranty period.

For assistance contact your nearest Rockland Sales Representative, or write to:

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West Nyack, New York 10994

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MODEL 5100 SPECIFICATIONS

FREQUENCY RANGE:	0.001 Hz to 2,000,000.000 Hz
FREQUENCY RESOLUTION:	0.001 Hz throughout entire range

INTERNAL CRYSTAL

TEMPERATURE STABILITY:	$\pm 2 \times 10^{-8}$/°C typical from 0° to 50°C
OPTION 01:	$\pm 2 \times 10^{-10}$/°C typical from 0° to 50°C
AGING RATE:	1 part in 10^8 per day; 1 part in 10^6 per year
OPTION 01:	1 part in 10^9 per day
EXTERNAL REFERENCE:	Accepts external 1 MHz or 8 MHz reference with TTL levels. Loading is one standard TTL load. Rear panel BNC jack.

OUTPUT SIGNALS

1 MHz REFERENCE OUTPUT:	Square wave with TTL levels capable of driving 30 standard TTL loads. Rear panel BNC jack.
FIXED OUTPUT:	Approximately 1 volt P-P with 50-ohm source impedance. Front and rear panel BNC jacks.
VARIABLE OUTPUT:	10 volts P-P maximum with 50-ohm source impedance. Front and rear panel BNC jacks.
ATTENUATOR:	Provides from 0 to 85 db attenuation of the variable output signal in steps of 1db. Front panel pushbutton control.
OPTION 02:	Attenuator operates either from front panel or remote program control.
LEVEL CONTROL:	Continuous control of the variable output signal from zero volts to full output at any given attenuator setting.

VARIABLE OUTPUT SIGNAL	0.001Hz	100kHz	500KHz	2MHz
RMS FRACTIONAL DEVIATION 10msec averaging 1 sec averaging		5×10^{-7} 5×10^{-9}		
PHASE NOISE In 30KHz band excluding 1 Hz centered on carrier		-50db		
SPURIOUS COMPONENTS	-70db	-60 db		-50 db
HARMONIC COMPONENTS At 1 volt RMS output At full output	 -55 db -55 db	 -50 db -50 db		 -45 db -40 db
FREQUENCY RESPONSE (full output) No load 50 ohm load		±.25 db ±.25 db		±.5 db +.5, -2.5 db
ATTENUATOR RESPONSE (to 60 db)		±.5 db		See Figure 2.2

REMOTE PROGRAMMING

FREQUENCY SELECTION: 31 bits in BINARY or 37 bits in BCD format. Format selected by one control bit.

ATTENUATION SELECTION: (Option 02) 7 bits (40,20,10,8,4,2,1 db).

LOADING SEQUENCE: Synchronous loading of all frequency and attenuation bits in one parallel word, or in four 12-bit bytes. Sequence selected by one control bit.

REMOTE MODE SELECTION: Via front panel push button or one control bit. Front panel lamp indicates remote mode.

PROGRAMMING DELAY: 1.5usec for BINARY-WORD with phase and amplitude continuity maintained.

20usec for BCD-WORD with output reset to zero phase during delay.

20usec minimum for four BCD or BINARY bytes with output reset to zero phase during programming.

UPDATE RATE:	625 nsec for BINARY-WORD mode 18 usec for BCD-WORD and BYTE modes
ZERO PHASE RESET:	Output signal may be asynchronously reset to zero phase via one control bit. There is a delay of approximately 800 nsec to the output. This line may also be used as a load acknowledge output.

ELECTRICAL AND PHYSICAL

OPERATING TEMPERATURE:	0°C to + 50°C ambient.
STORAGE TEMPERATURE:	-20°C to +70°C.
POWER REQUIREMENTS:	115 or 230 volts AC, ±10% 50-60 Hz, 65 watts.
SIZE:	3-1/2" H x 17"W x 13"D
WEIGHT:	21 lbs. Shipping weight 25 lbs.
ACCESSORIES SUPPLIED:	Rack adaptors, programming connector, and instruction manual.

OPTIONS

OPTION 01:	HIGH STABILITY REFERENCE. (Proportional Oven Control)
TEMPERATURE STABILITY:	$\pm 2 \times 10^{-10}$/°C from 0° to 50°C.
AGING RATE:	1 part in 10^9 per day.
OPTION 02:	REMOTELY PROGRAMMABLE ATTENUATOR
RANGE	0 to 85db in steps of 1 db.
PROGRAMMING DELAY	Typically less than 5msec.

1.0 INSTALLATION AND THEORY OF OPERATION

1.1 INSPECTION

This instrument was carefully inspected and tested prior to shipment. It was operated for at least 100 hours to reduce the probability of early failure. The instrument should be inspected for physical damage incurred in transit. When receiving a shipment from a carrier, inspect the shipping carton in the presence of the carrier. If rough handling is evident take exception on the delivery receipt before accepting the shipment.

If no carton damage is obvious, but physical damage is discovered when the carton is opened, preserve the carton and packing materials, notify the carrier immediately and have them perform a written inspection of the carton and the contents.

It is recommended that conformance to specifications be verified upon receipt. In case of discrepancies, refer to the warranty in this manual.

1.2 POWER REQUIREMENTS

This instrument will operate from 115 vac (±10%) 50-60 Hz, or 230 vac (±10%) 50-60 Hz, selectable via a rear panel switch. The instrument is equipped with a three-wire power cable which connects the chassis to earth ground when plugged into a three-contact outlet. If a two-contact outlet is used in conjunction with a three-prong and two-prong adaptor, the pigtail of the adaptor should be connected to earth ground.

1.3 INSTALLATION

The Model 5100 Frequency Synthesizer was factory assembled for bench use. To convert the instrument for mounting into a standard 19" wide rack, the following procedure should be followed. (Refer to Figure 1.1 throughout procedure.)

1. Unplug instrument from AC power source.
2. Remove Top and Bottom Covers (A) and (B) (screws on rear panel).
3. Remove Top and Bottom Support Strips (C) and (D). Note: Front panel (FP) will be loose but will not fall out.
4. Place instrument on flat surface in normal operating position.
5. Remove Main PC Board self-tapping support screws located on bracket along inside left side of instrument.
6. Stand instrument on right side.
   NOTE: Do not place undue stress on unsupported Main PC Board.
7. Remove single screw on rear panel and remove side frame of instrument, (E).

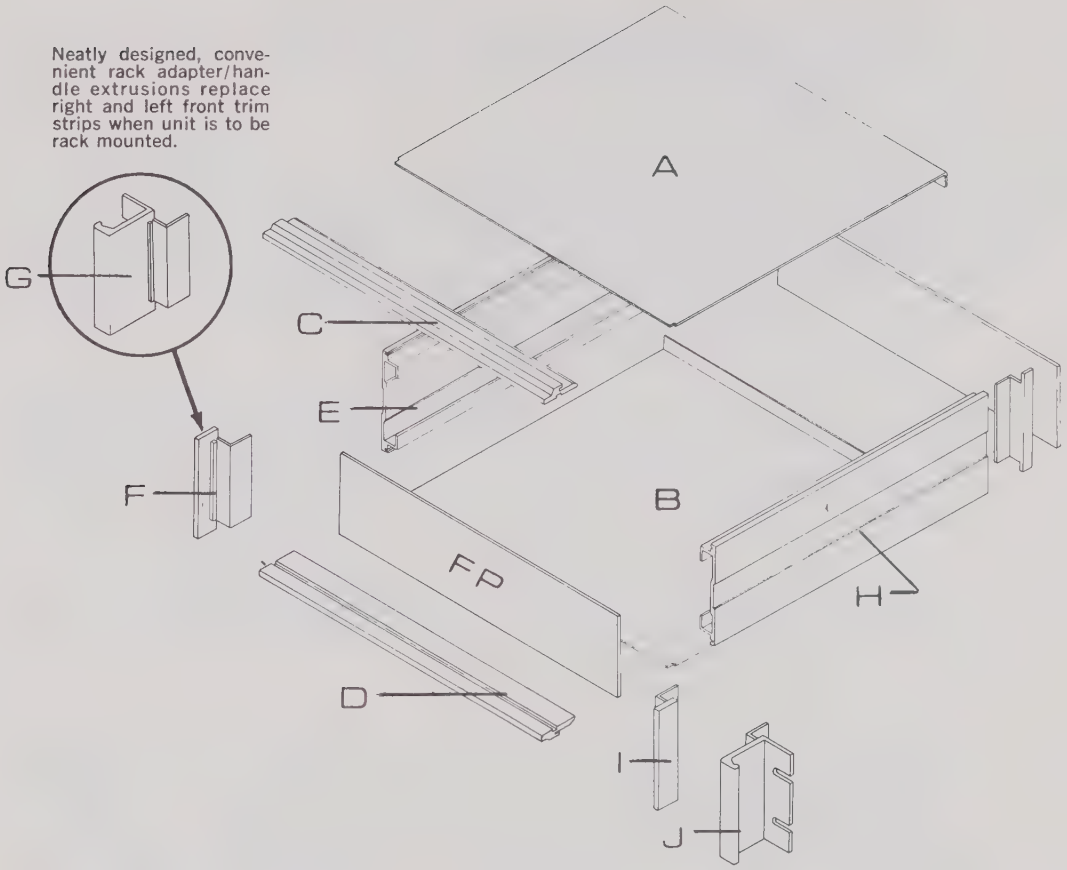


Figure 1.1 Model 5100 Chassis

8. Remove Front Side Bracket (F) from Left Side (E) and replace with Left Side Rack Adaptor Bracket (G), using same hardware.
9. Replace Left Side (E) making certain Front Panel (FP) is in retaining slot.
10. Replace Main PC Board support screws.
    CAUTION: DO NOT OVER-TIGHTEN SELF-TAPPING SCREWS.
11. Remove Main PC Board self-tapping support screws located on bracket along inside right of instrument.
12. Stand instrument on left side.
    NOTE: Do Not Place undue stress on unsupported Main PC Board.
13. Remove Right Side (H).
14. Remove Frontside Bracket (I) and replace with Right Side Rack Adaptor Bracket (J) using same hardware.

15. Replace Right Side (H) making certain Front Panel (FP) is in retaining slot.
16. Replace Main PC Board support screws.
    CAUTION: DO NOT OVER-TIGHTEN SELF-TAPPING SCREWS.
17. Replace Top and Bottom Support Strips (C) and (D).
18. Remove four (4) support feet and wire bail from Bottom Cover (B) and replace Cover on instrument.
19. Replace Top Cover (A).

Instrument is now ready for rack installation.

1.4 THEORY OF OPERATION

The Model 5100 utilizes direct digital synthesis techniques to generate the output sinusoid. Samples of the sinusoid are digitally generated at an 8MHz rate and are then converted to analog form by a Digital-to-Analog Converter (DAC) and a smoothing Low Pass Filter (LPF) cutting off at approximately 2.5 MHz. The amplitude of the digital samples is represented with 11 bits (including sign), and the phase accuracy of each sample is ±0.09°.

A block diagram of the Model 5100 is given in Figure 1.2. The 8 MHz system clock is derived from a temperature-compensated Crystal-Oscillator Reference (proportional oven control with Option 01), and the frequency stability of the output sinusoid is thus related directly to that of the crystal oscillator. Mechanical adjustment of the crystal frequency is provided to compensate for long-term aging effects, and the crystal oscillator may also be phase locked to an external 1 MHz reference (which is within ±2 Hz of the internally derived 1 MHz.) Since excellent short-term stability is provided by the internal crystal reference, the function of the external-reference phase-lock loop is only to provide proper bias to the crystal, and hence, the loop bandwidth is fairly broad ($\sim$ 10Hz).

The frequency of the output sinusoid is stored in the Frequency Register in binary form with each 3-decade group (KHz, Hz, and mHz) represented by a separate 10-bit binary number. A separate flip-flop stores the MHz bit. If the unit is remotely programmed in this binary form, then no numerical conversion is required, and the output frequency changes with no discontinuity in phase or amplitude. The delay from the programming inputs to the analog output in this mode is approximately 1.5 usec.

If the unit is programmed in BCD either locally (via the front panel) or remotely, then BCD-to-Binary conversion is required, and the output is reset to zero phase (and thus zero volts) during the conversion period. Remote programming in either BCD or binary can also be accomplished in four 12-bit bytes, (10 bits for binary) if the number of input lines is more important than programming speed.

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK

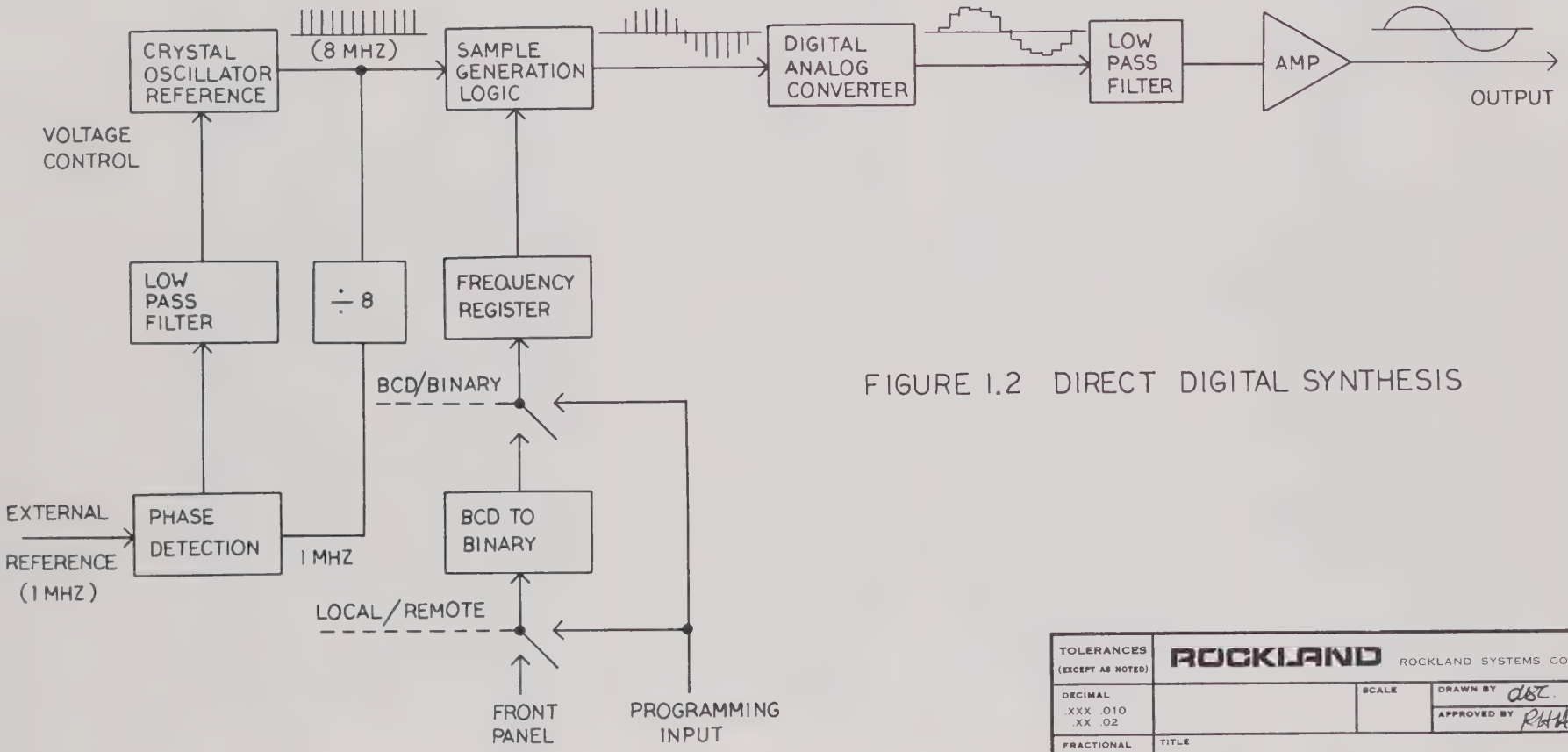


FIGURE 1.2 DIRECT DIGITAL SYNTHESIS

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP.		
DECIMAL .XXX .010 .XX .02		SCALE	DRAWN BY dst. APPROVED BY RHH
FRACTIONAL ± 1/64	TITLE DIRECT DIGITAL SYNTHESIS		
ANGULAR ±	DATE 2-28-72	DRAWING NUMBER	REV

2.0 OPERATING PROCEDURES

Figure 2.1 shows the front and rear panels of the instrument with functional controls identified in the key. The instrument may be controlled locally with the front panel switches or remotely via the rear panel programming connector. Frequency is programmable on all units, while attenuation is programmable on Option -02 units only.

2.1 REMOTE SWITCH and INDICATOR

The instrument is always operating in either the LOCAL or REMOTE mode as indicated by the amber REMOTE lamp on the front panel. The REMOTE switch must be in the OUT position for LOCAL mode operation. REMOTE mode operation may be effected in two ways:

1) by setting the REMOTE switch to the IN position and/or,

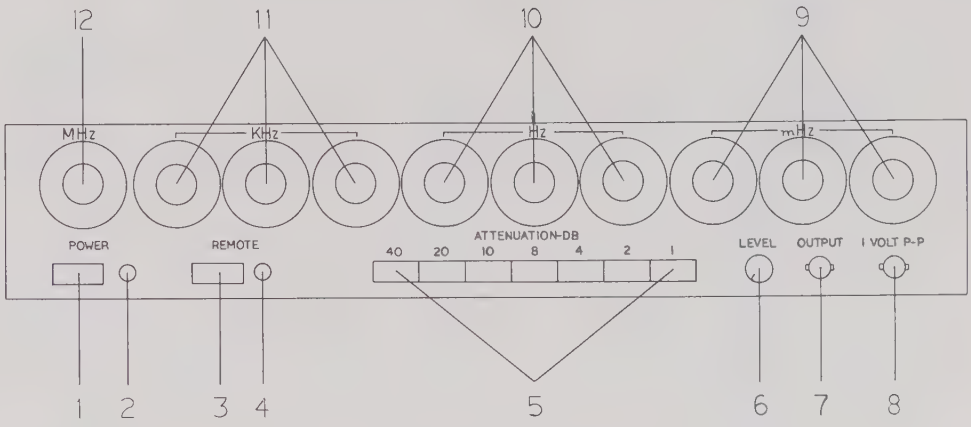
2) by setting the programming line REMOTE to the proper state. Thus, the unit may be called into the REMOTE mode by either front- or rear-panel control, and LOCAL mode operation requires that neither of (1) or (2) above be present.

2.2 LOCAL MODE OPERATION

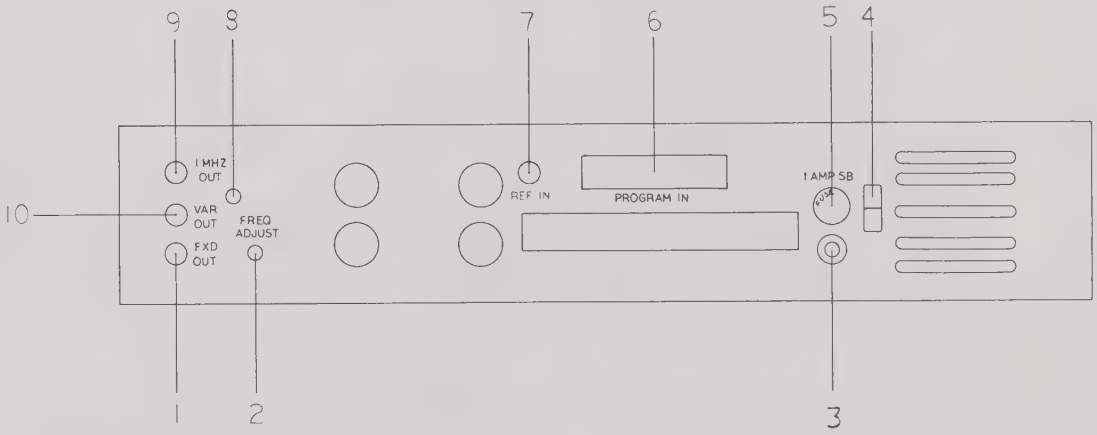
All frequency and attenuation control is derived from the front panel switches.

2.2.1 LOCAL FREQUENCY CONTROL

The output signal frequency is set directly by the ten front panel rotary switches. Any frequency from 0.001 Hz to 2,000,000.000 Hz is available in increments of 0.001 Hz. All switches (except the MHz switch) have 12 positions with no stops to limit rotation. The two unmarked positions on the knobs which correspond to "10" and "11" are actually valid positions with the following



1. POWER SWITCH
2. POWER INDICATOR
3. REMOTE SWITCH
4. REMOTE MODE INDICATOR
5. ATTENUATOR SWITCHES
6. LEVEL CONTROL
7. OUTPUT SIGNAL JACK
8. 1 VOLT P-P SIGNAL JACK
9. mHz FREQUENCY SWITCHES
10. Hz FREQUENCY SWITCHES
11. KHz FREQUENCY SWITCHES
12. MHz FREQUENCY SWITCH



1. 1 VOLT P-P SIGNAL JACK
2. STANDARD CRYSTAL ADJUST
3. LINE CORD
4. LINE SELECTOR SWITCH
5. FUSE HOLDER
6. PROGRAMMING JACK
7. EXT REFERENCE INPUT
8. HIGH STABILITY CRYSTAL ADJUST
9. 1 MHz REFERENCE OUTPUT
10. OUTPUT SIGNAL JACK

FIGURE 2.1 FRONT AND REAR PANELS

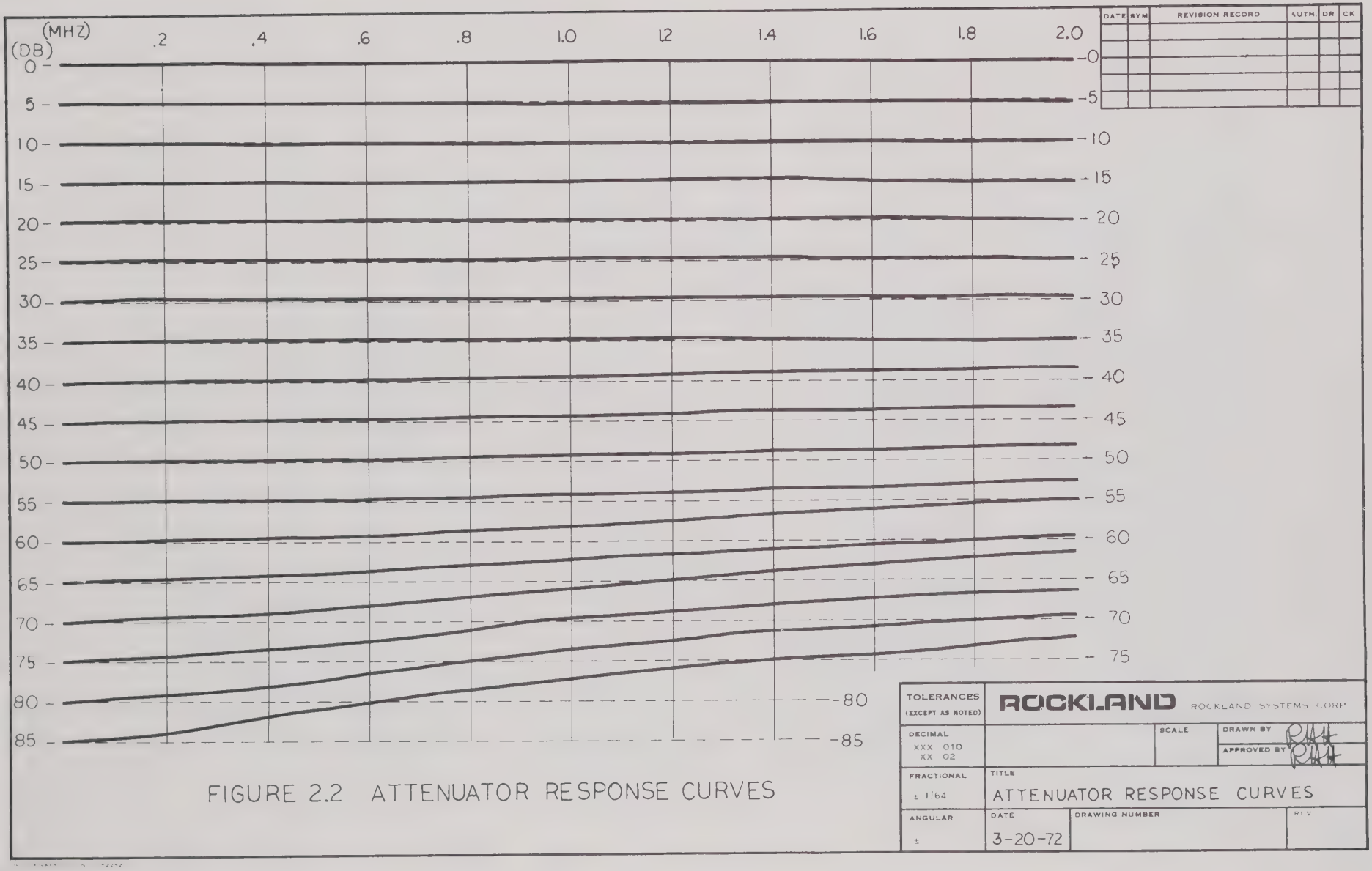
restrictions: the combined settings of the three switches in each range of 1000 (mHz, Hz, and KHz) may not exceed 999. For example, if the three "Hz" switches are set left to right as "8", "10", "11", the output frequency is given by: "8" x 100 + "10" x 10 + "11" x 1 = 911 Hz. An example of an invalid setting for the same three switches is "9", "10", "11" which totals 1011 Hz, exceeding the limit of 999.

The MHz switch is a two position switch. To set the frequency 2,000,000.000 Hz, the MHz switch is set to 1 and the 100KHz switch is set to "10". This is the only frequency which requires the use of an unmarked switch position.

When any frequency switch is changed, the output signal will momentarily drop to zero volts DC before the new frequency appears. The duration of this so-called "ZERO PHASE" portion depends primarily on the bounce time of the switch contacts but will be 13.5usec minimum. The new frequency waveform will always start at zero phase.

The ATTENUATION switches on the front panel may be used to attenuate the OUTPUT signal from 0 to 85 db in steps of 1db. Any combination of switch settings is valid; the total attenuation is equal to the total of the weights of the switches set to the IN position. There is some degree of rolloff of attenuation at the higher frequencies. Figure 2.2 shows the actual attenuation as a function of frequency.

The LEVEL control affords continuous amplitude control of the OUTPUT signal from zero volts to the full output at any given attenuator setting. An out-



DATE	SYM	REVISION RECORD	AUTH.	DR	CK

FIGURE 2.2 ATTENUATOR RESPONSE CURVES

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP		
DECIMAL XXX .010 XX .02		SCALE	DRAWN BY RMK APPROVED BY RMK
FRACTIONAL ± 1/64	TITLE ATTENUATOR RESPONSE CURVES		
ANGULAR ±	DATE 3-20-72	DRAWING NUMBER	REV

put impedance of 50 ohms is maintained over all ATTENUATION and LEVEL control settings. The maximum amplitude of the OUTPUT jack is 10 volts P-P. The jack labeled VAR OUT on the rear panel provides the same signal.

2.2.3 1 VOLT P-P OUTPUT

The front and rear panel jacks labeled 1 VOLT P-P and FXD OUT, respectively, provide a reference sinewave signal which may be used for scope synchronization or frequency monitoring. The output impedance is 50 ohms and the open circuit amplitude is approximately 1 volt P-P, independent of the LEVEL and ATTENUATION control settings.

2.3 REMOTE MODE OPERATION

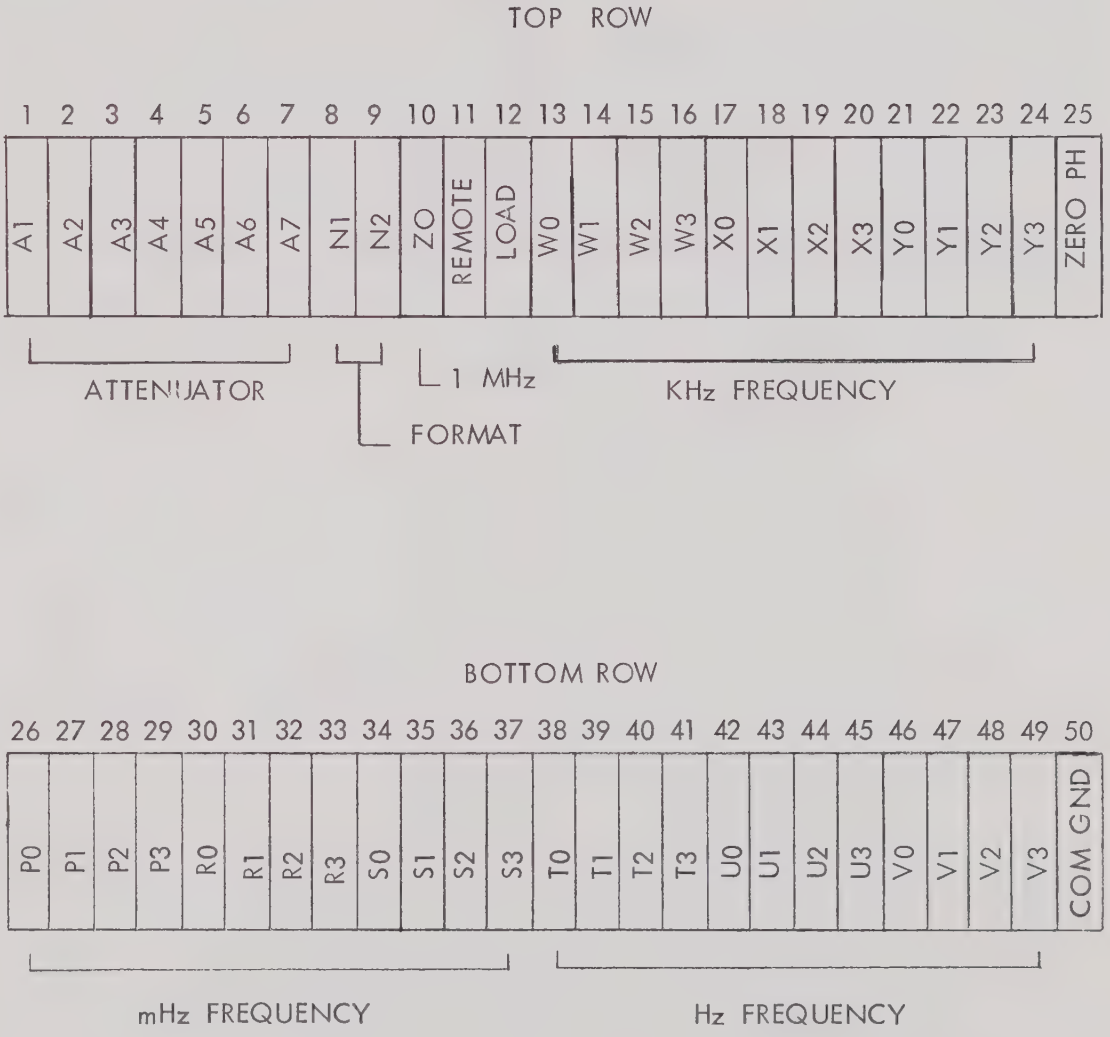
The programmable functions of this instrument are frequency, zero-phase point, and with Option-02, attenuation. Programming data is latched internally at the time of the LOAD pulse and need not be held valid except at that time. The precise switching characteristics of this instrument allow accurate amplitude gating, frequency sweeping, and frequency hopping (FSK).

2.3.1 Programming Lines

All remote programming lines enter the 50-pin connector on the rear panel. The pin numbers shown on the connector and its mating plug (supplied) are identified in Figure 2.3. Lines A1 through A7 determine the attenuation (Option -02 only); N1 and N2, the loading format; and P_0 through Y_3 and Z_0, the frequency. REMOTE, LOAD, and ZERO PHASE lines are control lines.

All lines require positive logic with standard TTL levels: logical "0" is from 0.0 volts to 0.8 volts and logical "1" is from 2.0 volts to 5.5 volts, all

Figure 2.3 Rear Panel Programming Connector - Rear View


TOP ROW
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
A1 A2 A3 A4 A5 A6 A7 N1 N2 ZO REMOTE LOAD W0 W1 W2 W3 X0 X1 X2 X3 Y0 Y1 Y2 Y3 ZERO PH
ATTENUATOR
1 MHz
FORMAT
KHz FREQUENCY
BOTTOM ROW
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
P0 P1 P2 P3 R0 R1 R2 R3 S0 S1 S2 S3 T0 T1 T2 T3 U0 U1 U2 U3 V0 V1 V2 V3 COM GND
mHz FREQUENCY
Hz FREQUENCY

Notes:

1. All signals are referenced to pin 50 COM GND.
2. All lines are internally pulled to +5V by 3.3 Kohm resistors and assume logical "1" level if unconnected.
3. See figure 2.4 for Programming Chart.

referenced to the GND line. If left unconnected, a line will assume a logical "1" condition and therefore may be programmed via contact closure to ground for logical "0" and open for logical "1".

2.3.2 REMOTE Line

As described in section 2.1, the instrument may be called into the REMOTE mode either by the REMOTE switch on the front panel or via the programming line REMOTE. With this line in the logical "1" state, REMOTE/LOCAL mode selection is determined by the REMOTE switch; in the logical "0" state, the instrument is in the REMOTE mode, regardless of the position of the REMOTE switch.

2.3.3 ZERO PHASE Line

This line may be used both as an input and as an output. As an input, the line is normally at logical "1". By setting a logical "0" on this line, the internal sample generator is reset to the zero-phase state causing the output signal to go to zero volts DC. When this line is set back to logical "1", the output waveform resumes at the zero-phase point. The minimum duration of the logical "0" interval is 125 nsec, and there is approximately 1.5 usec delay to the OUTPUT jack.

The instrument may be used to generate an amplitude gate waveform by driving the ZERO PHASE line with a pulse generator; each gated interval is identical in phase content. All transients are spectrally limited to a 2.5 MHz bandwidth by the lowpass smoothing filter.

Every time the instrument changes frequency (except with phase-continuous programming), the internal circuitry causes the ZERO PHASE line to go to logical

"0" during the processing time of the newly-loaded data. Thus, as an output, this line may be used to monitor the internal status of the data processing circuitry.

The ZERO PHASE line is electrically similar to a DTL "wired-or" bus. Internally, it is pulled to +5V through a 1K ohm resistor and to ground through a saturated NPN transistor capable of sinking 200ma. Externally, it may be pulled to logical "0" through a low impedance path to ground (switch, diode, transistor, etc.) and may be set to logical "1" by opening this path.

2.3.4 LOAD Line

The LOAD line is used to transfer programming data from the programming lines into the internal data register. This line is normally at logical "1" and the falling edge of a negative-going pulse causes a load. The positive-going edge is ignored with the restriction that the pulse width is 50nsec minimum.

2.3.5 Data Formats

There are four basic formats for loading data: BINARY-WORD, BCD-WORD, BINARY-BYTE, and BCD-BYTE. The format is programmable via bits N1 and N2 which are entered along with other data at the time of the LOAD pulse. The WORD mode permits loading of all data with a single load pulse while BYTE mode allows the user with a limited number of programming lines to load four 12-bit bytes sequentially. The weights of the lines may be either BCD or BINARY. Each of the four modes is described below and summarized in Figure 2.4.

2.3.5.1 BINARY WORD

In this mode, N1=N2=logical "0" as shown in the MODE SELECT column

in Figure 2.4. All lines are loaded with a single load pulse. The weight of each program line is shown beneath each line designation. Positive logic is used: a logical "1" on any of the lines will cause a contribution to the frequency equal to the weight of that line. Any binary number less than or equal to $999_{10} = 1111100111_2$ is valid for each of the three frequency ranges (KHz, Hz, and mHz). The lines Y_2, Y_3, V_2, S_2 and S_3 are unused in this mode and may be left unconnected. Any lines which are always to be logical "0" are simply hardwired to GND.

The BINARY-WORD mode is the only programming mode which maintains phase and amplitude continuity between frequencies. Frequency sweeping is easily accomplished by causing repetitive loads of successively higher (or lower) frequencies. Although the frequency changes in discrete steps, each step can be as small as 0.001 Hz allowing a close approximation to a linear sweep in most applications.

The delay from the negative edge of the LOAD pulse to the change in frequency at the OUTPUT jack is approximately 1.5usec. LOAD pulses may be accepted at a maximum rate of one per 0.625usec. Data must be held valid until at least 0.625us after the negative edge of the LOAD pulse. The ZERO PHASE line is logical "1" during all BINARY-WORD loads. These conditions are indicated on the timing diagram in Figure 2.5.

2.3.5.2 BCD-WORD

In this mode, N1= logical "0" and N2= logical "1". Programming lines are weighted in BCD code and are analogous in format to the front panel frequency

switches. The total of the weights in any of the three ranges (KHz, Hz, and mHz) cannot exceed 999 ; otherwise, any combination of weights is valid. For example, the frequency 150 Hz could be programmed with several different sets of data: (1) 100 Hz + 40 Hz + 10 Hz, (2) 100 Hz + 40 Hz + 8 Hz + 2 Hz, (3) 80 Hz + 40 Hz + 20 Hz + 10 Hz, etc. By properly choosing data lines, the number of active programming lines may be minimized in certain applications.

Data must remain valid for at least 4.5 usec after the negative-going edge of each LOAD pulse. The internal data processing circuitry requires a maximum of 18.0 usec to process the BCD data after a load. During the last 13.5 usec of this interval, the ZERO PHASE line will go to zero volts. The instrument is ready to receive a new load after this time, as shown in Figure 2.5.

2.3.5.3 BCD-BYTE and BINARY-BYTE

The byte loading mode is provided expressly for the user who has a limited number of data lines. Four 12-bit bytes are required, each byte being loaded in 12-bit parallel form. The first byte loads the MODE SELECT bits (N1 and N2), the ATTENUATOR bits (A1 through A7, Option -02 only) and the 1 MHz bit (Z_0) on the lines shown in Figure 2.4. A LOAD pulse causes loading of this data and initiates a wait cycle holding the ZERO PHASE line (and OUTPUT signal) at zero until the next three bytes have been loaded and processed. Data must be held valid for at least 4.5 usec after the first LOAD pulse.

The remaining three bytes program the mHz, Hz and KHz in that order, as shown in Figure 2.4. Each range (mHz, Hz, and KHz) is constrained exactly as in the word modes. The fourth LOAD pulse initiates processing of all loaded data after which the new signal appears at the output jacks. Data must be held valid for at least 375 nsec after each of the last three LOAD pulses.

Since the first byte and the remaining three bytes are loaded on two separate sets of lines, the user may tie these two sets in parallel, allowing a single set of 10 or 12 lines to serve for all byte inputs. These sets of lines are arranged adjacent to each other on the rear panel connector (see Figure 2.3) so that pins #1 through #10 may be easily connected to pins #26 through #35, respectively. Pins #36 and #37 are then included with the above ten lines to form a total of twelve for BCD bytes. Note that if binary format is used, these latter two lines may be omitted thus requiring a total of only ten lines for data input.

2.3.6 REMOTE ATTENUATION

If Option -02 has been installed, attenuation of the OUTPUT signal as described in section 2.2.2 is fully programmable. The source of control (LOCAL or REMOTE) is the same as that for the frequency. The format is shown in Figure 2.4, and loading of the attenuation bits occurs at the same time as the frequency bits. Internal registers store the data and drive miniature relays to switch the appropriate resistor networks. The settling time of the relay contacts is typically less than 5 msec.

Protective circuitry insures that when switching between two levels of attenuation, the settling of the relays will never cause attenuation less than either of the two valid levels.

2.3.7 REMOTE-LOCAL MODE TRANSITIONS

The characteristics of switching between LOCAL and REMOTE modes may be useful in some applications. When switching from LOCAL to REMOTE modes no change occurs in frequency (or attenuation) until the first LOAD pulse is received. If, however, at the time of entering the REMOTE mode the LOAD line is at logical "0", the instrument will thereupon load the program data. In order to load new data either the LOAD line must go to logical "1" and then back to logical "0", or the instrument must go to LOCAL mode and back to REMOTE mode. Whenever LOCAL mode is entered, the instrument immediately returns to the current front panel setting. Therefore, if the user wishes to switch between two frequencies he could set the first on the front panel and the second on the program lines. With the LOAD line at logical "0", switching between LOCAL and REMOTE modes would then alternate the frequencies. The transition into LOCAL mode is identical in character to a BCD-WORD load and the timing diagram of Figure 2.5 applies, substituting the REMOTE condition for the LOAD signal.

Another application may require transitions from one frequency to another without the relatively complex amplitude and frequency transients encountered in rotating the front panel switches to change frequency. This may be done on the front panel without resorting to remote programming. To change frequency, enter the REMOTE mode with the REMOTE button and set the frequency switches to the new frequency. Changing the switches will have no effect. Push the REMOTE button, again bringing the instrument back to LOCAL mode. The frequency will change to the new setting. This routine is equivalent to remote programming

in the BCD-WORD mode.

With Option -02, the attenuator may be controlled in the same manner as the frequency setting described above.

2.4 1 MHz OUT

The rear panel jack labeled 1 MHz OUT provides a buffered TTL square-wave output derived from the internal reference. This signal is capable of driving up to 30 standard TTL loads.

2.5 EXTERNAL SYNCHRONIZATION

There are two modes of external synchronization. The internal 8 MHz clock may be phase-locked to an external 1 MHz standard or it may be replaced directly by an external 8 MHz clock signal.

2.5.1 PHASE-LOCKING TO EXTERNAL 1 MHz STANDARD

The clock jumper shown in figure 5.1 must be in the INT position. A 1 MHz signal is connected to the REF IN jack on the rear panel. The pull-in range of the phase-locked loop is ± 2 Hz. The waveform of the input signal must enter the limits of logical "0" and logical "1" (each for a duration of at least 50 nsec) once for each cycle. A Schmitt-trigger circuit conditions the signal before it enters the phase-locked loop. The absolute maximum voltage limits are ± 5.5 volts.

As a check of proper phase-lock operation, follow section 3.7 of the Conformance Test Procedure. Failure to lock could be due to an excessive difference between the internal and external reference frequencies.

Two or more instruments may be phase-locked to each other by connecting the 1 MHz OUT signal of one (master) instrument directly to the REF IN jack of the other (slave) instrument(s). The clock jumper must be in the INT position.

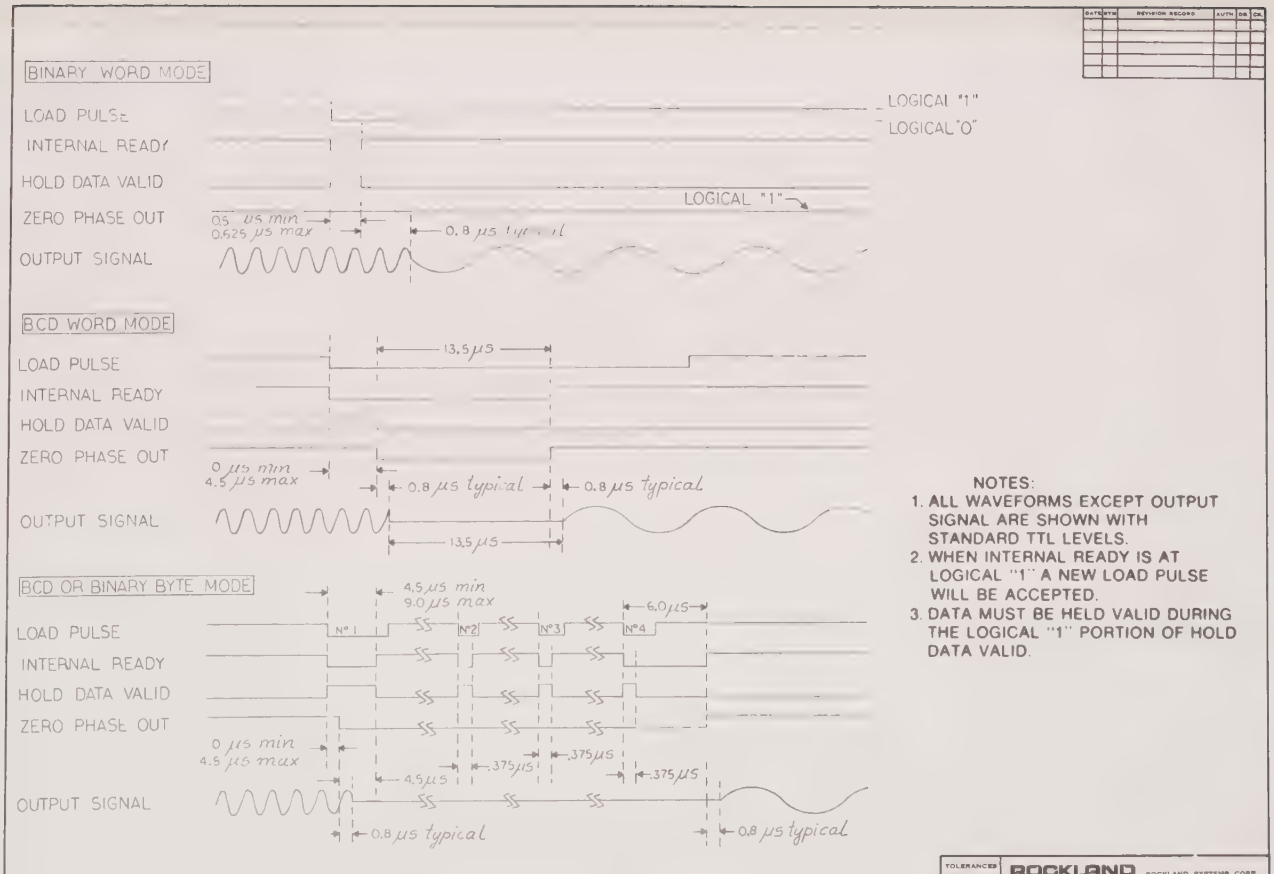
2.5.2 EXTERNAL 8 MHz CLOCK

The clock jumper shown in figure 5.1 must be in the EXT position. An 8 MHz signal is connected to the REF IN jack on the rear panel. The waveform and voltage limits are the same as for the 1 MHz signal above. The input is conditioned by a Schmitt trigger.

The frequency limits of this signal are from DC to 8.1 MHz. The deviation of the frequency of the output signal is directly proportional to the deviation of the external clock from 8 MHz. Operation at frequencies below 8 MHz implies a lower sampling rate; the internal low pass filter which removes sampling components from the output signal is designed for an 8 MHz sampling rate and becomes ineffective as the sampling rate is lowered. To maintain full harmonic and spurious distortion specifications, an external low pass filter is required to eliminate these components.

DATE	BY	REVISION RECORD	AUTH	DR.	CK.

| MODE | MODE SELECT | | ATTENUATOR | | | | | | | FREQUENCY | | | | | | |



NOTES:

1. ALL WAVEFORMS EXCEPT OUTPUT SIGNAL ARE SHOWN WITH STANDARD TTL LEVELS.
2. WHEN INTERNAL READY IS AT LOGICAL "1" A NEW LOAD PULSE WILL BE ACCEPTED.
3. DATA MUST BE HELD VALID DURING THE LOGICAL "1" PORTION OF HOLD DATA VALID.

FIGURE 2.5

ROCKLAND ROCKLAND SYSTEMS CORP.

TITLE: TIMING DIAGRAM - LOADING

DRAWING NUMBER: 510406

REV: A

3.0 CONFORMANCE TEST PROCEDURE

This section describes procedures for verifying correct operation of the instrument and for making the necessary adjustments for optimum performance. If faulty operation is suspected, the steps in this section should be followed to determine the origin of the problem. Section 4 of this manual contains a trouble shooting routine which is keyed to the steps in section 3. After each conformance test in section 3, there is a reference in parenthesis to a trouble shooting (TS) chart in section 4.

Equipment required in the procedure is described below:

1. VARIAC (variable autotransformer) - Voltage range = 0 to LINE, current = 1 amp.

2. OSCILLOSCOPE - Wideband (25 MHz), multi-channel (two channels minimum), vertical sensitivity = 20mV/cm, triggered sweep.

3. VOM - capable of AC and DC voltage readings, 20,000 ohms/volt on DC.

4. RMS VOLTMETER - Calibrated in db, reads from +20dbm to -80dbm.

5. FREQUENCY COUNTER - Range 1 Hz to 2 MHz with 1 sec gating interval. Must accept 10 volt P-P sinewave.

See section 4.1.6 for description of part designations and IC socket numbering.

3.1 POWER SUPPLY

Equipment required for this test: VOM, Variac, and oscilloscope. Refer to figures 5.2, 5.8.1, and 5.8.2 for test points, component locations and schematic.

3.1.1 Initial Conditions VARIAC: Dial set at 0 volts.

3.1.2 Initial Conditions 5100: Line cord connected to VARIAC, power ON, LOCAL mode, frequency setting = 0 Hz.

3.1.3 Connect negative probe of meter to ground bus at point A. Connect positive probe to point B and increase setting of VARIAC until a reading of +2.0 volts DC is reached. (TS 4.2.1)

3.1.4 Move positive probe to point C and verify +5 volts DC (TS 4.2.1)

3.1.5 Move negative probe to point D, positive probe to point E and verify +5 volts DC. (TS 4.2.1)

3.1.6 Move negative probe to point A and positive probe to point B. Increase setting of VARIAC gradually, watching the meter climb to approximately +9 volts DC at full line voltage. (TS 4.2.1)

3.1.7 Initial conditions Scope: vertical sensitivity = 1 volt/cm, DC coupled, free running sweep. Connect ground lead of scope probe to point A.

3.1.8 Connect tip of scope probe to points F, G, and H, reading 5.0 volts DC at each point. The trace must be "clean" with a maximum noise component of 200mV P-P. (TS 4.2.2)

3.1.9 Set vertical sensitivity to 5 volts/cm on scope. Connect tip of probe to point J and verify +15 volts DC with 200 mV maximum noise. (TS 4.2.2)

3.1.10 Connect tip of probe to point K and measure -15 volts DC with 200mV maximum noise. (TS 4.2.2)

3.2 FRONT PANEL DATA

Equipment required: Oscilloscope. Refer to figures 5.2 and 2.1 for part locations. S1 thru S10 are front panel frequency switches right to left.

3.2.1 Initial Conditions 5100: Power ON, LOCAL mode, frequency setting = 0Hz.

3.2.2 Initial Conditions Scope: Vertical Sensitivity = 5 volts/div, DC coupled, sweep = .5usec/cm, sync triggered on negative slope of Channel A.

3.2.3 Connect Ch A probe to point DC and verify a negative pulse waveform with a width of 40nsec and a period of 4.5 usec. (TS 4.2.3)

3.2.4 Adjust position and sweep controls on scope so that the positive-going edges of two consecutive pulses are aligned with the first and the ninth vertical division lines. See figure 3.1.

3.2.5 Connect Ch B probe to FPD (Front Panel Data). Signal should be logical "1". (TS 4.2.5)

3.2.6 The FPD waveform on Ch B represents the setting of the front panel switches S1 through S9 in BCD code, serial form. Negative logic is used so that the logical "1" condition in 3.2.5 reflects the 0 Hz setting. With the scope adjusted as per 3.2.4, the first division of FPD represents S1, the second division S2, etc. Within each of the nine divisions there are four subdivisions corresponding to the $\overline{1}$-$\overline{2}$-$\overline{4}$-$\overline{8}$ code for each switch, left to right.

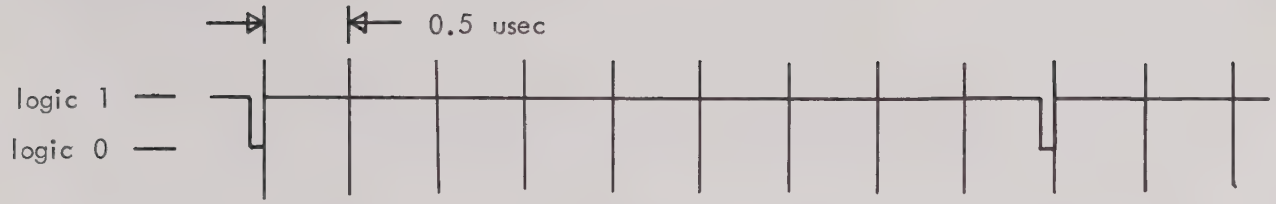


Figure 3.1 Waveform at point DC ($\overline{DCLK}$) as in 3.2.4.

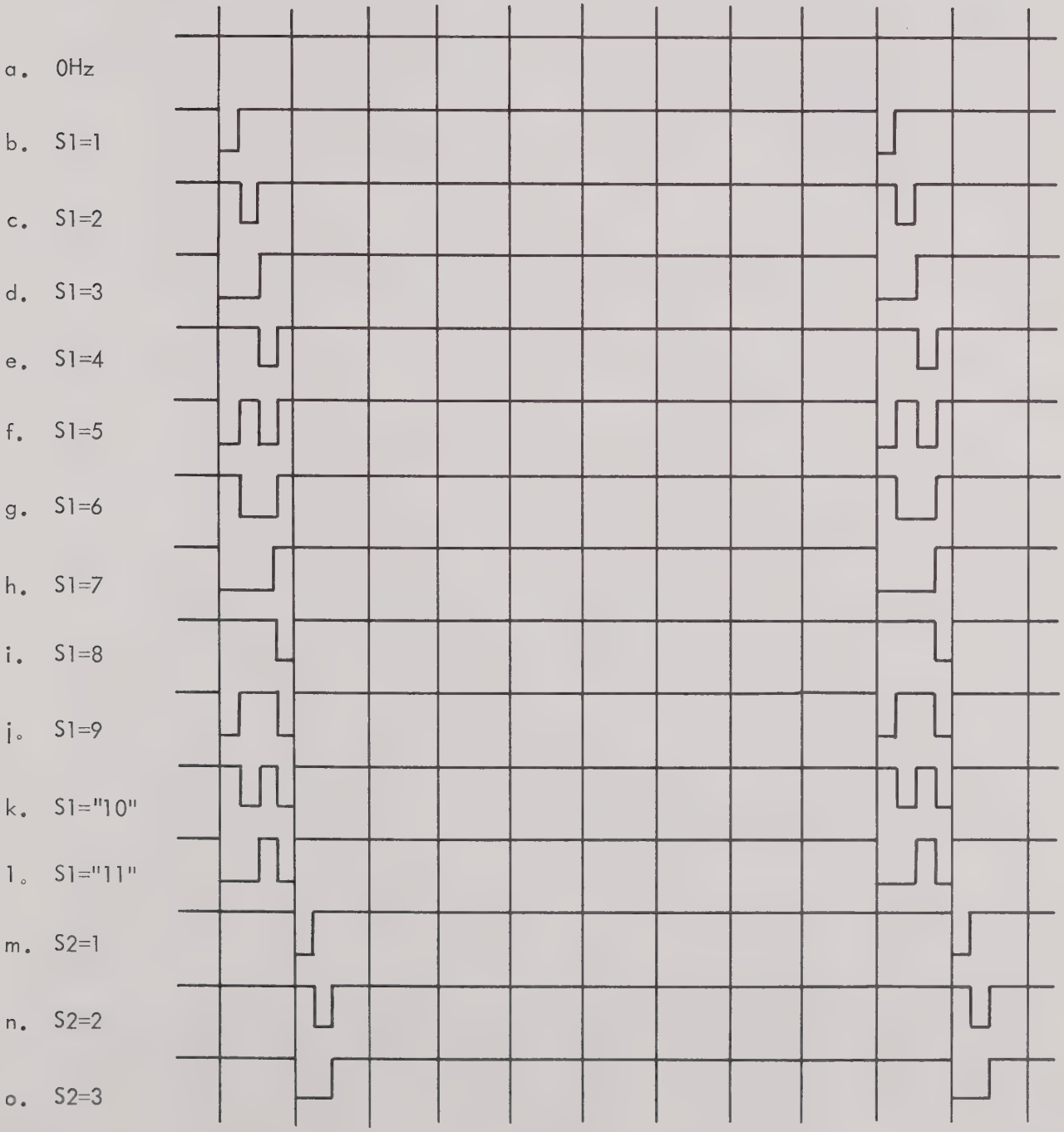


Figure 3.2 Waveform for FPD as described in 3.2.7 and 3.2.8.

3.2.7 Rotate S1 through its twelve positions verifying the negative-logic BCD code in the first division of FPD as described in 3.2.6. See figures 3.2 a through 3.2 l. (TS 4.2.7).

3.2.8 Repeat 3.2.7 for switches S2 through S9. See figures 3.2 m through 3.2 o , etc. (TS 4.2.7).

3.3 SAMPLE GENERATOR

Equipment required: Oscilloscope: Refer to figures 5.1 and 5.2 for D/A converter location and test points.

3.3.1 Initial Conditions 5100: LOCAL mode, Frequency set to 4KHz, power ON.

3.3.2 Initial Conditions Scope. vertical sensitivity = 5 volts/cm , DC coupled, sync triggered on positive slope of Ch A.

3.3.3 Connect Ch A probe to DAC-1 and verify a square-wave with a period of 250 usec. (TS 4.2.6)

3.3.4 Adjust sweep of scope to set one full cycle of the square wave in 3.3.3 to fill 10 horizontal divisions. See figure 3.3.a.

3.3.5 Connect Ch B probe to DAC-2 and verify waveform in figure 3.3.b. (TS 4.2.8).

3.3.6 If more than two channels are provided on the scope, connect them to consecutive DAC pins allowing easier comparison between signals. If only two channels are available, Ch B will have to be checked against Ch A only.

3.3.7 Display the signal on DAC-3 and compare with figure 3.3.c. (TS 4.2.8)

3.3.8 Display the signals on DAC-4 through DAC-11 and compare with figures 3.3.d through 3.3.k . (TS 4.2.9)

3.4 DC OFFSET ADJUSTMENT

Equipment required: Oscilloscope. Refer to figure 5.1 for location of parts.

DATE	SYM	REVISION RECORD	AUTH.	DR	CK.

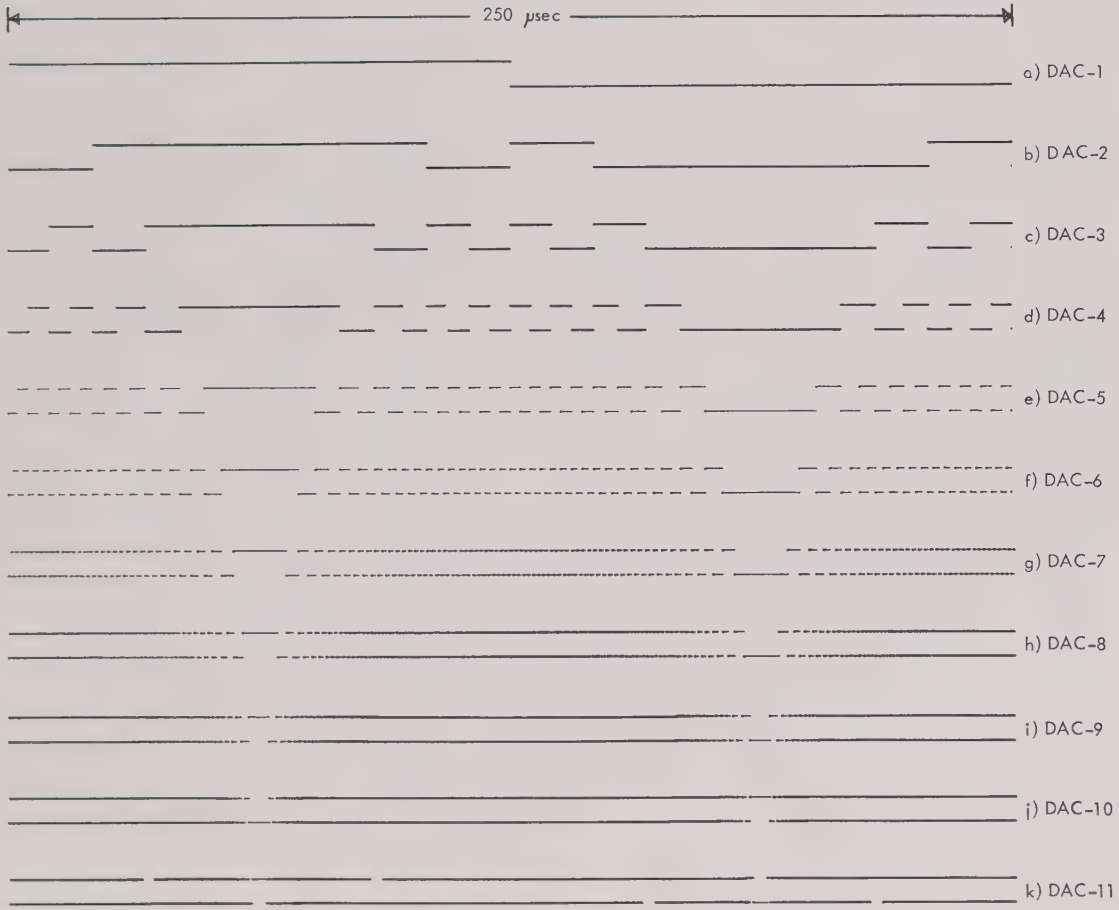


FIGURE 3.3 SAMPLE WAVEFORM GENERATOR

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP.		
DECIMAL .XXX .010 .XX .02		SCALE	DRAWN BY RHH APPROVED BY RHH
FRACTIONAL ± 1/64	TITLE SAMPLE WAVEFORM GEN		
ANGULAR ±	DATE 3-2-72	DRAWING NUMBER	REV

3.4.1 Initial Conditions 5100: Power ON, LOCAL mode, frequency setting = 0 Hz, LEVEL control fully CCW.

3.4.2 Initial Conditions Scope: DC coupled, vertical sensitivity = 20mv/cm, free-running sweep.

3.4.3 Connect OUTPUT signal of 5100 to scope. Adjust R29 for minimum DC voltage. (TS 4.2.15).

3.4.4 Set LEVEL control fully CW. Adjust R19 for minimum DC voltage. (TS 4.2.15).

3.5 FRONT PANEL FREQUENCY

Equipment Required: Frequency Counter. Refer to figure 5.2 for component locations. S1 through S10 are the ten front panel frequency switches numbered right to left.

3.5.1 Initial Conditions: Power ON, LOCAL mode, 0 Hz frequency setting.

3.5.2 Connect frequency counter to OUTPUT signal to monitor frequency, 1 second gate interval.

3.5.3 Rotate S4 from position 0 through position 9 verifying the correct frequency on the counter. (TS 4.2.7).

3.5.4 Repeat step 3.5.3 with switches S5 through S9. (TS 4.2.7).

3.5.5 Remove the Hz CARRY jumper shown in figure 5.1. Connect the blue mHz CARRY jumper supplied in the plastic bag from point MT to point MC.

3.5.6 Repeat step 3.5.3 with S1, S2, and S3 reading the frequency on the counter in Hz for a setting of mHz on the 5100. (TS 4.2.7).

3.5.7 Remove the blue mHz CARRY jumper and replace the small, black Hz CARRY jumper.

3.5.8 Set S10 to 1 MHz and S1 through S9 to 0 Hz. Read 1 MHz on the counter. (TS 4.2.11).

3.6 REMOTE MODE

Equipment required: Frequency counter, oscilloscope, and a programming unit capable of setting all data lines to logical "1" or logical "0" as directed. A bounceless LOAD pulse is required. In the procedure below this programming unit is referred to as PGM. Refer to section 2 of this manual for detailed REMOTE loading instructions. All lines are assumed to be logical "0" unless specified.

3.6.1 Initial Conditions on 5100:

a. Power ON.
b. LOCAL mode.

3.6.2 Connect PGM to rear panel connector.

3.6.3 Set PGM to REMOTE. Verify REMOTE lamp on front panel is lit. (TS 4.2.4b).

3.6.4 Connect 5100 OUTPUT signal to frequency counter with 1 second gate interval.

3.6.5 Set PGM to BINARY-WORD and load logical "1"'s for frequency bits corresponding to 1Hz through 512KHz one at a time, checking the frequency on the counter after each load. (TS 4.2.12).

3.6.6 Set PGM to BCD-WORD and repeat step 5 with lines corresponding to 1 Hz through 800KHz. (TS 4.2.12).

3.6.7 Remove the Hz CARRY jumper shown in figure 5.1. Connect the blue mHz CARRY jumper supplied in the plastic bag from point MT to point MC.

3.6.8 Set PGM to BINARY-WORD and load logical "1"'s for frequency lines corresponding to 1mHz through 512mHz, one at a time. The frequency counter should indicate readings of 1Hz through 512Hz. (TS 4.2.12)

3.6.9 Set PGM to BCD-WORD and repeat step 3.6.8 with lines corresponding to 1mHz through 800mHz. (TS 4.2.12).

3.6.10 Set PGM to BINARY-BYTE. Set PGM mHz lines to (512 + 128 + 32 + 8 + 2) and enter three LOAD pulses. Set mHz switches to (256 + 64 + 16 + 4 + 1) and enter one LOAD pulse. Counter should read 341,682 Hz. (TS 4.2.12).

3.6.11 Set PGM to BCD-BYTE. Set mHz lines to (400 + 100 + 40 + 10 + 4 + 1) and MHz line to 1. Enter three load pulses. Set mHz lines to (400 + 200 + 100 + 80 + 8 + 1) and enter one LOAD pulse. Counter should read 1,789,555 Hz. (TS 4.2.12)

3.6.12 Remove the blue jumper and replace the black jumper.

3.6.13 Set PGM to BINARY-WORD, LOCAL, 2KHz.
Set 5100 to LOCAL, 1KHz.
Connect OUTPUT to both frequency counter and oscilloscope.
OUTPUT should be 1KHz sinewave. Set PGM to REMOTE mode.
OUTPUT should not change. (TS 4.2.12).

3.6.14 Enter LOAD pulse. Verify OUTPUT frequency changes to 2KHz. (TS 4.2.12)

3.6.15 Set PGM to LOCAL mode. Verify OUTPUT frequency changes to 1KHz. (TS 4.2.12)

3.7 INTERNAL OSCILLATOR ADJUSTMENT

Equipment required: Oscilloscope, and an external 1 MHz frequency standard. The waveform of this signal is arbitrary but for each cycle it must enter the limits of logical "0" and logical "1" voltage levels. The absolute maximum limits are ±5 volts.

3.7.1 Initial conditions on 5100: Power ON, LOCAL mode, frequency Setting = 0 Hz, clock jumper in INT position. See Fig. 5.1.

3.7.2 Initial conditions on scope: vertical sensitivity = 5 volts/cm, sweep = 100nsec/cm, sync triggered on Ch A.

3.7.3 Connect external 1 MHz standard to Ch A of scope and adjust trigger to lock the waveform.

3.7.4 Connect the 1MHz OUT signal from the 5100 rear panel to Ch B. Verify a 1 MHz square wave. (TS 4.2.14)

3.7.5 Locate the proper FREQ ADJ hole on the rear panel. With a small, non-metallic flat-bladed screwdriver, adjust the slug so that the waveform of Ch B is stationary with respect to Ch A. (TS 4.2.14)

3.7.6 Connect the 1MHz standard to the REF IN jack on the rear panel of the 5100 and verify that the leading edges of the waveforms of Ch A and Ch B are phase-locked at 180°. (TS 4.2.14)

3.8 STANDARD ATTENUATOR

Equipment required: RMS Voltmeter.

3.8.1 Initial Conditions on 5100: Power ON, LOCAL mode, frequency = 1KHz, attenuation = 0db, LEVEL = fully clockwise.

3.8.2 Connect the meter to the OUTPUT jack and verify a reading of greater than + 13 dbm. Note this reading as the 0db reference point.

3.8.3 Add attenuation in steps of 1 db from 0db to 85db and verify the attenuation relative to the reference point. Attenuation error must lie within the limits of -.5, +0 db up to 60 db and -2.0, +0 db up to 85 db.

3.9 PROGRAMMABLE ATTENUATOR

Equipment required: RMS Voltmeter, and a programming unit (like the unit described in 3.6) capable of setting the attenuator data lines to logical "0" or logical "1" as directed.

3.9.1 Follow steps 3.8.1 through 3.8.3 and verify LOCAL mode operation. (TS 4.2.16).

3.9.2 Set 5100 with REMOTE mode. Set PGM to BINARY-WORD and 1KHz.

3.9.3 Enter and load logical "1"'s on lines A1 through A7 one at a time, verifying the correct attenuation on the meter within the limits specified in 3.8.3. (TS 4.2.16).

4.0 TROUBLE SHOOTING

In the event of a malfunction, a mechanical inspection is advised before proceeding with the trouble shooting section. Inspect all IC's for proper seating in each socket; check proper insertion of the two plug-in PC cards in the connector sockets.

4.1 INSTRUCTIONS FOR USE OF THE TROUBLE SHOOTING CHART

4.1.1 If trouble develops, start with the CONFORMANCE TEST PROCEDURE (CTP) in section 3, following it until a discrepancy is found. Refer to the TS (Trouble Shooting) section which appears in parenthesis after the non-conforming item and start trouble shooting at this section in the TROUBLE SHOOTING CHART.

4.1.2 Set up the TEST CONDITIONS, connect the appropriate instrument to the TEST POINT and verify results in each OBSERVATION row. If the OBSERVATION description is verified, continue downward to the next OBSERVATION, changing TEST CONDITIONS and TEST POINT as necessary.

4.1.3 If the OBSERVATION is not verified, refer to the REMEDY column in that row. Perform each part of the REMEDY instructions one at a time and recheck the results with the OBSERVATION column until OBSERVATION checks.

4.1.4 When the results are corrected, return to the CTP and recheck the test which failed previously. If the test still fails, return to the TROUBLE SHOOTING CHART and resume testing with the LAST step performed above.

4.1.5 If the trouble is not found after exhausting the steps within one section, do not continue into the next section. Rather, return to theCTP and repeat all tests made to that point, hopefully uncovering some earlier discrepancy not noticed before.

4.1.6 a. Part designations may be found on the assembly drawings in section 5. The assemblies are numbered as follows:

A 1	-	Main PC Board (Motherboard) Assembly
A 2	-	Front Panel Scanner Board Assembly
A 3	-	Attenuator Board Assembly
A 4	-	Front Panel Assembly
A 5	-	Rear Panel Assembly

All part designations on Assembly A 1 will have no prefix, while parts on A2, A3, A4, A5 will have designations with these prefices.

4.1.6 b. Designations for pins on IC sockets are in the form UXX-YY where XX is the IC socket number and YY is the pin number. Pin numbers for TOP views of the three sizes of IC package used are shown in figure 4.2.

4.1.6 c. IC socket numbers on Assemblies A 1 and A2 are etched into bottom side of the PC board.

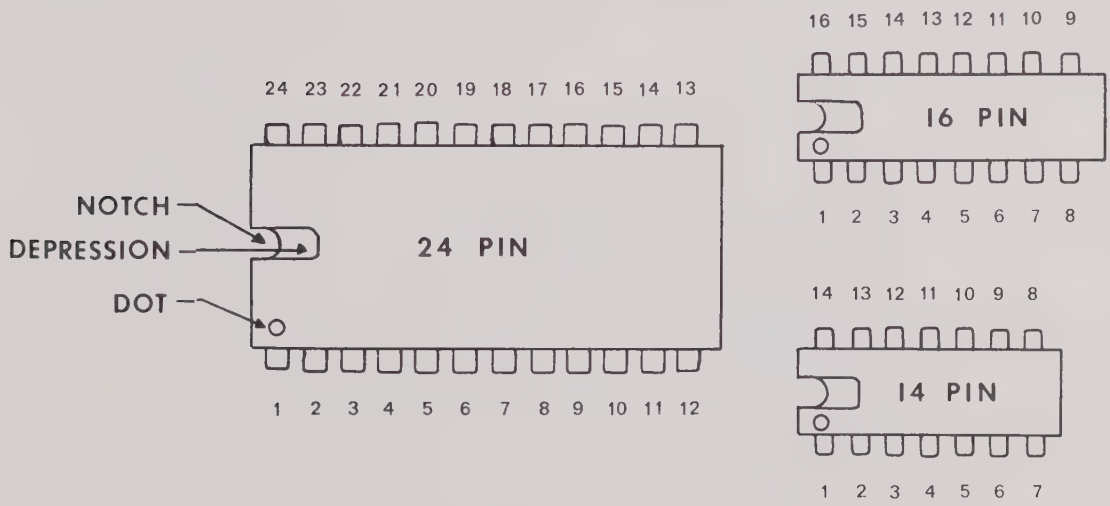


Figure 4.2 DIP Pin Numbering

4.2 If the cause of the problem cannot be found, the factory should be consulted. A complete and accurate description of the problem should be made in order to help locate the cause. If the unit is to be returned to the factory, a written and pictorial report should be enclosed to aid in duplicating the operating conditions under which the unit failed.

ROCKLAND SYSTEMS CORPORATION
230 West Nyack Road
West Nyack, New York 10994
Phone: (914) 623-6666
TWX: 710-575-2631

4.2.1 Low or Unregulated Digital Supply Voltage

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Power OFF		Check fuse	Replace if necessary
1. Power ON 2. Apply 5VAC across line cord (10VAC for units that are switched to 230VAC line power by the power selection switch on the back panel)	A5T1 PRI #1 0-115	Measure 5VAC	Check continuity of line cord, fuse holder, and power switch S2B. Replace if defective.
	A5T1 PRI #2 0-115	Measure 5VAC	
	A5T1 SEC #1 0-8	Measure 0.4VAC	1. If voltages are all zero, replace XFORMER A5T1. 2. If one or more voltages are low, check for shorts or opens in wiring to bridge rectifiers. 3. Check bridge rectifiers A5CR1, CR2, CR3.
	A5CR1 - AC Input		
	A5T1 SEC #2 0-16.5	Measure 0.75VAC	
	CR2 AC Input		
	A5T1 SEC #3 0-16.5	Measure 0.75VAC	
	CR3 AC Input		
	Across C1	Measure 0.8VDC	1. Check for shorted C1, C2, C3, Q1, Q2, Q3 and replace.
	Across C6	Measure 0.8VDC	1. Check for shorted C6, Q4, and replace.
	Across C7	Measure 0.8VDC	1. Check for shorted C7, Q5, and replace.

4.2.2 Low or Zero Regulator Voltage

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Power ON 2. Normal line voltage	F	As per CTP 3.1.8	Replace Q3
	G	As per CTP 3.1.8	Replace Q2
	H	As per CTP 3.1.8	Replace Q1
	J	As per CTP 3.1.9	Replace Q4
	K	As per CTP 3.1.10	Replace Q5

4.2.3 No $\overline{\text{DCLK}}$ at Test Point DC See Figure 5.3 for timing signals.

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. LOCAL mode.	U96-1	8MHz pulse waveform	Check power supply voltages. Replace XTAL oscillator Y1.
2. Power ON 3. Clock jumper to INT position	U7-6	Negative pulse waveform. $\overline{\text{CLK}}$. Width=40nsec; Period=125nsec.	Replace U97, U89, U70, U81, U96
	U6-8	Negative pulse waveform. $\overline{\text{ACLK}}$. Width=40nsec; Period=125nsec.	Replace U6, U7, U8, U9, U22
	U18-8	Negative pulse waveform. $\overline{\text{BCLK}}$. Width=40nsec; Period=500nsec.	Replace U5, U4, U18, U70.
	U18-6	Negative pulse waveform. $\overline{\text{CCLK}}$. Width=40nsec; Period=1.5usec.	Replace U17, U18, U19.
	U19-6	Negative pulse waveform. $\overline{\text{DCLK}}$. Width=40nsec; Period=4.5usec.	Replace U29, U18, U19, U53.
	U19-8	Negative pulse waveform. $\overline{\text{ECLK}}$. Width=40nsec; Period=4.5usec.	Replace U19, U10.

4.2.4 (a) REMOTE Lamp Always ON

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. REMOTE button in OUT position.	U22-1	Logical "1"	Programmer is causing REMOTE mode. Check programming.
	U22-2	Logical "1"	1. Replace U22, U10. 2. Test and replace S-2A if necessary.
	U10-9	Logical "0"	Replace U10, U19, U70.

4.2.4 (b) REMOTE Lamp Always OFF

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
REMOTE button in IN position.	U22-3	Logical "1"	1. Replace U22, U10. 2. Test and replace S-2A if necessary.
	U70-11	Logical "0"	Replace U19, U10, U70.
			Replace L1.

4.2.5 Incorrect Static Front Panel Data Stream

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. LOCAL mode.	J1-19	Negative pulse waveform. $\overline{ACLK}$ Width=40nsec; Period=125nsec	Replace U97, A2U1 thru A2U8, A2U10, Go to Section 4.2.3.
2. 0Hz FP Setting.	J1-12	Logical "1"	Replace U10, A2U3. Go to Section 4.2.4 (a).
3. Scope Sync as per 3.2.4 of CTP.	A2U9-8	Negative pulse waveform. $\overline{A4 \cdot B3 \cdot C3}$ Width=125nsec; Period=4.5usec.	Replace A2U9. Verify C3 on J1-1 and A4·B3 on J1-2.
	J1-10	Logical "1"	Replace A2U4 through A2U8 until J1-10 is logical "1".

4.2.6 Sample Generator Malfunction

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. LOCAL mode	U98-11	Negative pulse waveform Width=40nsec; Period=125nsec.	Replace U97, U89, U96, go to 4.2.3.
2. 4KHz FP Setting	U25-10	Negative pulse waveform Width=40nsec; Period=125nsec.	Replace U97
	U104-9	Logical "1"	1. Verify A5J1-25 (ZERO PHASE) is logical "1". If not, correct it. 2. Replace U79, U104, U50.
1. .001 Hz FP Setting	Pins #12 to 15 on U12, U23, U35, U46, U55 U63, U72, U80 Pins #13 to 15 on U1.	Logical "0"	Go to Section 4.2.10
	U1-12	Logical "1"	
	U36-13	Positive pulse waveform. Width=125nsec; Period=125usec See Figure 5.4.	Replace U2, U13, U24, U15, U26, U25, U3, U14.
1. 1Hz FP Setting	Pins #12 to15 on U1, U12, U23, U46, U55 U63, U72, U80 Pins #13 to15 on U35.	Logical "0"	Go to Section 4.2.10
	U35-12	Logical "1"	
	U64-13	Positive pulse waveform. Width=125nsec; Period=125usec See Figure 5.4.	Replace U36, U47, U56, U38, U49, U25, U37, U48, U57.
1. 1KHz FP Setting	Pins #12 to15 on U1, U12, U23, U35, U46, U55, U72, U80, Pins #13 to15 on U63.	Logical "0"	Go to Section 4.2.10
	U63-12	Logical "1"	

4.2.6 (continued)

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1 KHz FP Setting	U58-5	Positive pulse waveform. Width=125nsec; Period=125usec. See Figure 5.4.	Replace U64, U73, U82, U66 U65, U74, U58, U84.
	U83-9	1 KHz square wave.	Replace U83, U95, U82.

4.2.7 Incorrect Front Panel Stream

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. LOCAL mode 2. Scope Sync as per 3.2.4 of CTP.	J1-10	As per CTP 3.2.7 or 3.2.8	Go thru Section 4.2.5 Replace A2U1 through A2U8 until data is correct.

4.2.8 DAC-1, 2, or 3 Incorrect

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Replace U85, U78, U86, U87, U88, U95, U90, U91, U92, U77, U68, U59, U67, U76, U84

4.2.9 DAC-4 through DAC-11 Incorrect

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Replace U90, U92, U93, U100, U101, U102, U103, U94.

4.2.10 Incorrect Frequency Register Contents

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Remove A2U10 (scanner ass'y) 2. LOCAL mode.	U53-12 or $\overline{D4}$.	Negative pulse waveform. $\overline{D4}$ Width=4.5usec; Period=18usec.	Replace U52, U44, U53, U19.
1. Sync on negative edge of U53-12 or $\overline{D4}$.	U60-8 U51-12 U51-6	Negative pulse waveform. Width=40nsec; Spacing=125nsec. Pulses blanked to logical "1" during logical "0" portion of U53-12. There are 108 pulses within a period of U53-12.	Replace U60, U51, U52, U61, U41, U40, U4.
	U70-6	Same as U53-12.	Replace U70, U62.
1. Sync on negative edge of U53-14 or $\overline{D2}$. 2. Set FP Switches to 555,555.555 Hz.	U1-12 or QH	Alternating "1010..." pattern during logical "0" portion of U53-14. One alternation per 125nsec. There are 18 "1"s and 18 "0"s.	Replace U39, U80, U72, U63, U55, U46, U35, U23, U12, U1. Check CTP Section 3.2.
1. Sync on negative edge of U53-13 or $\overline{D3}$. 2. Set FP Switches to 819,819.819 Hz.	U80-2 or K	Alternating "1010..." pattern during logical "0" portion of U53-13. One alternation per 250nsec. There are 9 "1"s and 9 "0"s.	Replace U32, U30, U43, U54, U44, U42, U33, U40.

4.2.11 1MHz Operation Incorrect

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. LOCAL mode. 2. 0 Hz Setting	U27-9	Logical "0"	Replace U27, U16.
1. 1 MHz Setting	U27-9	Logical "1".	
			Replace U82, U84, U83.

4.2.12 Remote Operation Incorrect

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Disconnect Programmer. 2. Connect jumper from U31-4 or LD to U53-10 or DC.	U10-5	Positive pulse waveform. Width=125nsec; Period-4.5usec.	Replace U31, U20, U10.
3. REMOTE mode. 4. Jumper from U34-7 or W to GND.			Replace U22, U9, U8, U7, U34, U4, U41.

4.2.13 No 1MHz Output

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Replace U81, U97.

4.2.14 Crystal Cannot Be Adjusted Into Proper Range.

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Replace U96, U98, U91, C13.
			Replace XTAL Y1.

4.2.15 Output Amplifier Defective

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
		Refer to the schematic in figure 5.7.1 for DC voltage test points, and verify these voltages.	Replace defective components.

4.2.16 Programmable Attenuator

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. LOCAL mode.	J2-4 or AC	Logical "1"	See Section 4.2.4.
	A3U8-14	+ 5 VDC	Replace A3Q1.
	A3U8-3 A3U8-6	Logical "0"	Replace A2U8.
1. Disconnect Programmer. 2. Connect jumper from U31-4 or LD to U53-10 or DC. 3. REMOTE mode 4. Jumper from U34-7 or W to GND.	A3U9-5	Negative pulse waveform. Width=125nsec; Period=4.5usec.	Replace A2U9.
Remove jumpers above. Test each attenuator bit in LOCAL and REMOTE modes as per CTP 3.9.		For errors in attenuation settings of: 1 db 2 db 4 db 8 db 10 db 20 db 40 db	Replace following parts on assembly A3: A3-U2, -U1, -U9, -K1 A3-U2, -U3, -U10, -K2 A3-U3, -U4, -U10, -K3 A3-U4, -U5, -U11, -K4 A3-U6, -U5, -U11, -K5 A3-U6, -U7, -U12, -K6 A3-U8, -U7, -U12, -K7

5.0 Schematic and Assembly Drawings

Figure No.	Title
5.1	Motherboard Assembly A1 - Component Side
5.2	Motherboard Test Points Assembly A1 - Bottom Side
5.3	Basic Timing Signals
5.3.1	Timing Section Schematic
5.4	Accumulator Signals
5.4.1	Accumulator Section Schematic
5.5	ROM Address Signals
5.5.1	DAC Section Schematic
5.6	Motherboard IC Parts List
5.6.1	IC Manufacturer Cross Reference List
5.7	Output Amplifier Parts List
5.7.1	Output Amplifier Section Schematic
5.8	Power Supply Parts List
5.8.1	Power Supply Assembly A5
5.8.2	Power Supply Section Schematic
5.9	Standard Attenuator Parts List
5.9.1	Standard Attenuator Assembly A3
5.9.2	Standard Attenuator Schematic
5.10	Programmable Attenuator Parts List
5.10.1	Programmable Attenuator Assembly A3
5.10.2	Programmable Attenuator Schematic
5.11	Front Panel Scanner Parts List
5.11.1	Front Panel Scanner Assembly A2
5.11.2	Front Panel Scanner Schematic

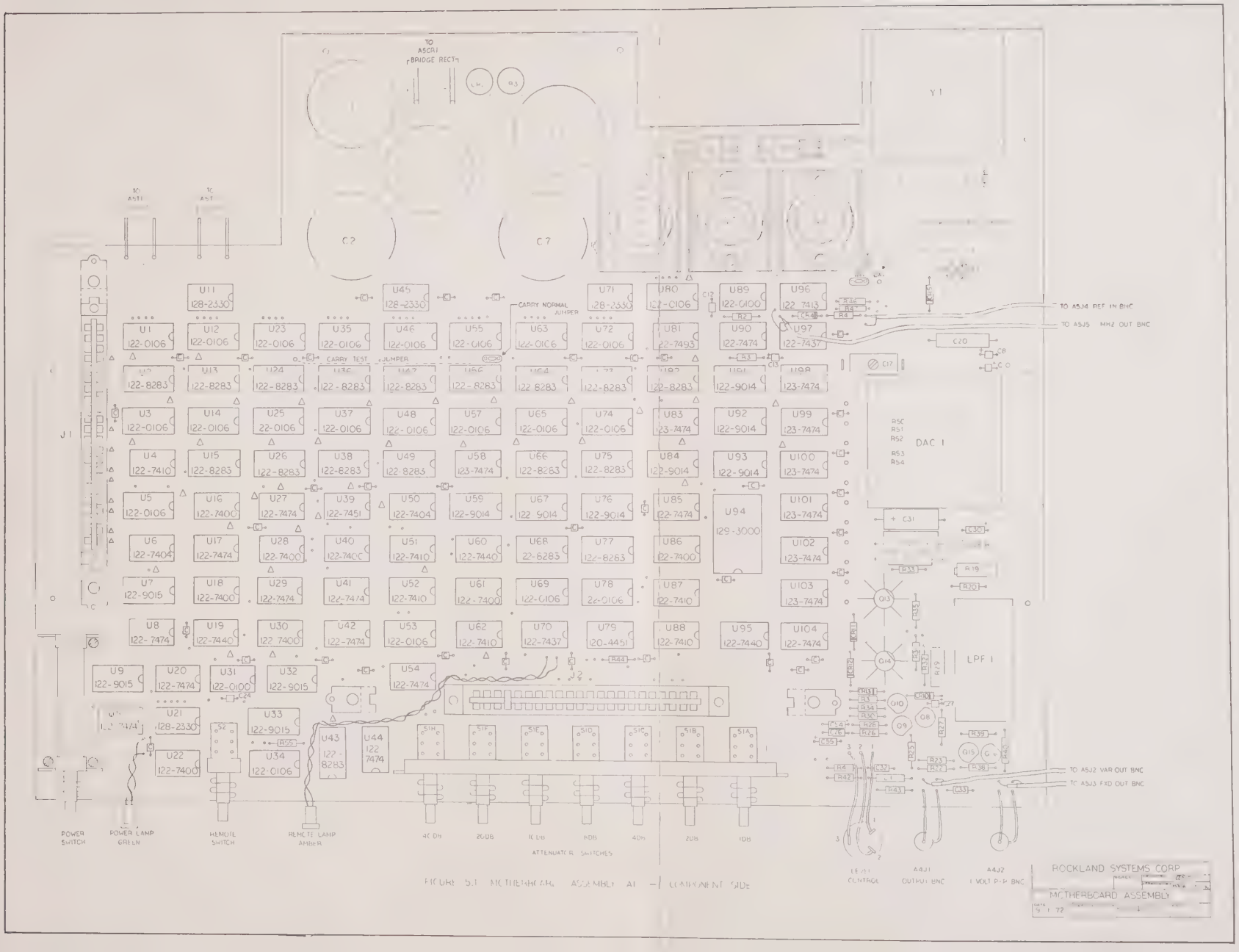


FIGURE 5-1 MOTHERBOARD ASSEMBLY A1 - COMPONENT SIDE

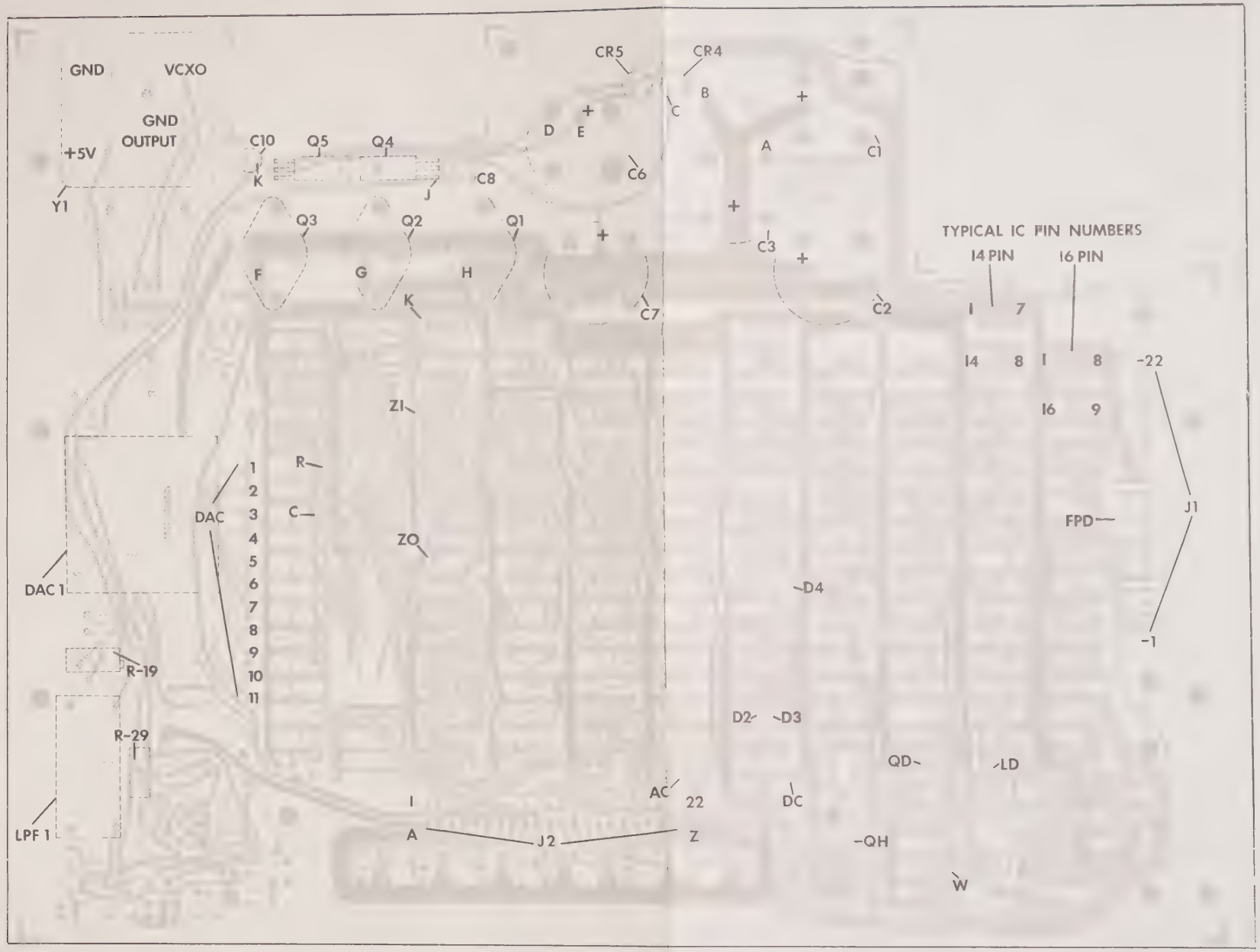


FIGURE 5.2 MOTHERBOARD ASSEMBLY A1 — BOTTOM SIDE

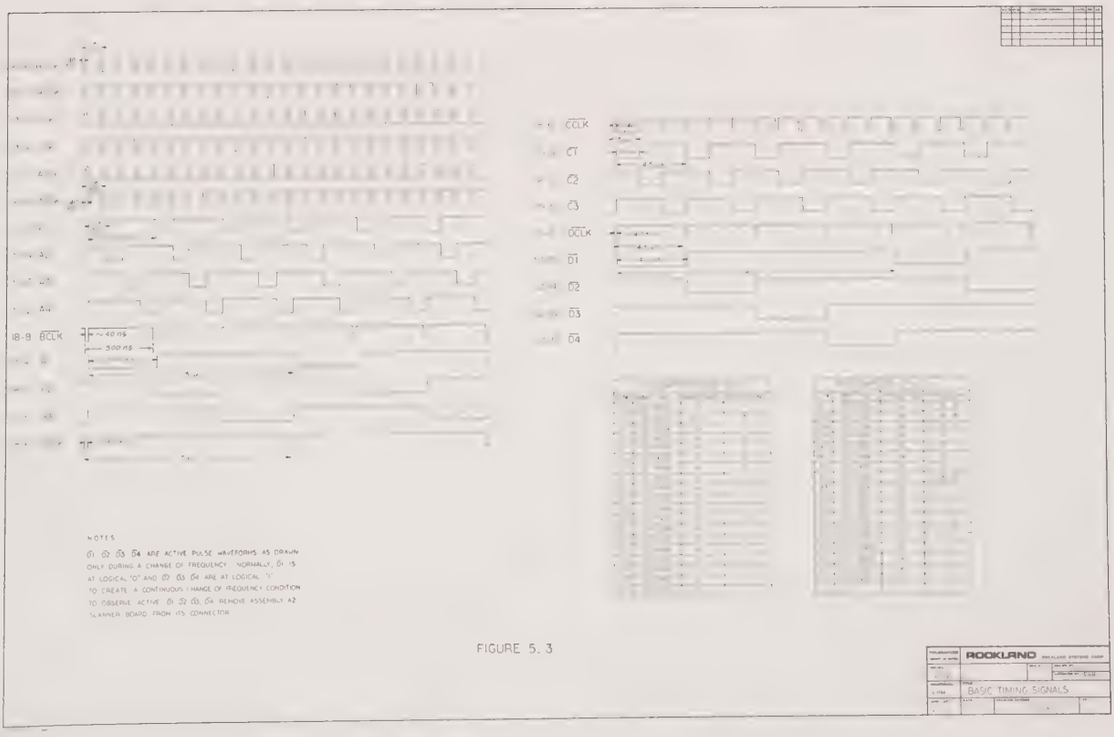

$\overline{CCLK}$
CT
$\overline{C2}$
$\overline{C3}$
$\overline{DCLK}$
$\overline{D1}$
$\overline{D2}$
$\overline{D3}$
$\overline{D4}$
18-9 $\overline{BCLK}$
F ~ 40 MS
300 MS
NOTES
$\overline{D1}$ $\overline{D2}$ $\overline{D3}$ $\overline{D4}$ ARE ACTIVE PULSE WAVEFORMS AS DRAWN ONLY DURING A CHANGE OF FREQUENCY. NORMALLY, $\overline{D1}$ IS AT LOGICAL "0" AND $\overline{D2}$ $\overline{D3}$ $\overline{D4}$ ARE AT LOGICAL "1".
TO CREATE A CONTINUOUS CHANGE OF FREQUENCY CONDITION TO OBSERVE ACTIVE $\overline{D1}$ $\overline{D2}$ $\overline{D3}$, $\overline{D4}$ REMOVE ASSEMBLY A2 SCANNER BOARD FROM ITS CONNECTOR
ROCKLAND
BASIC TIMING SIGNALS

FIGURE 5.3

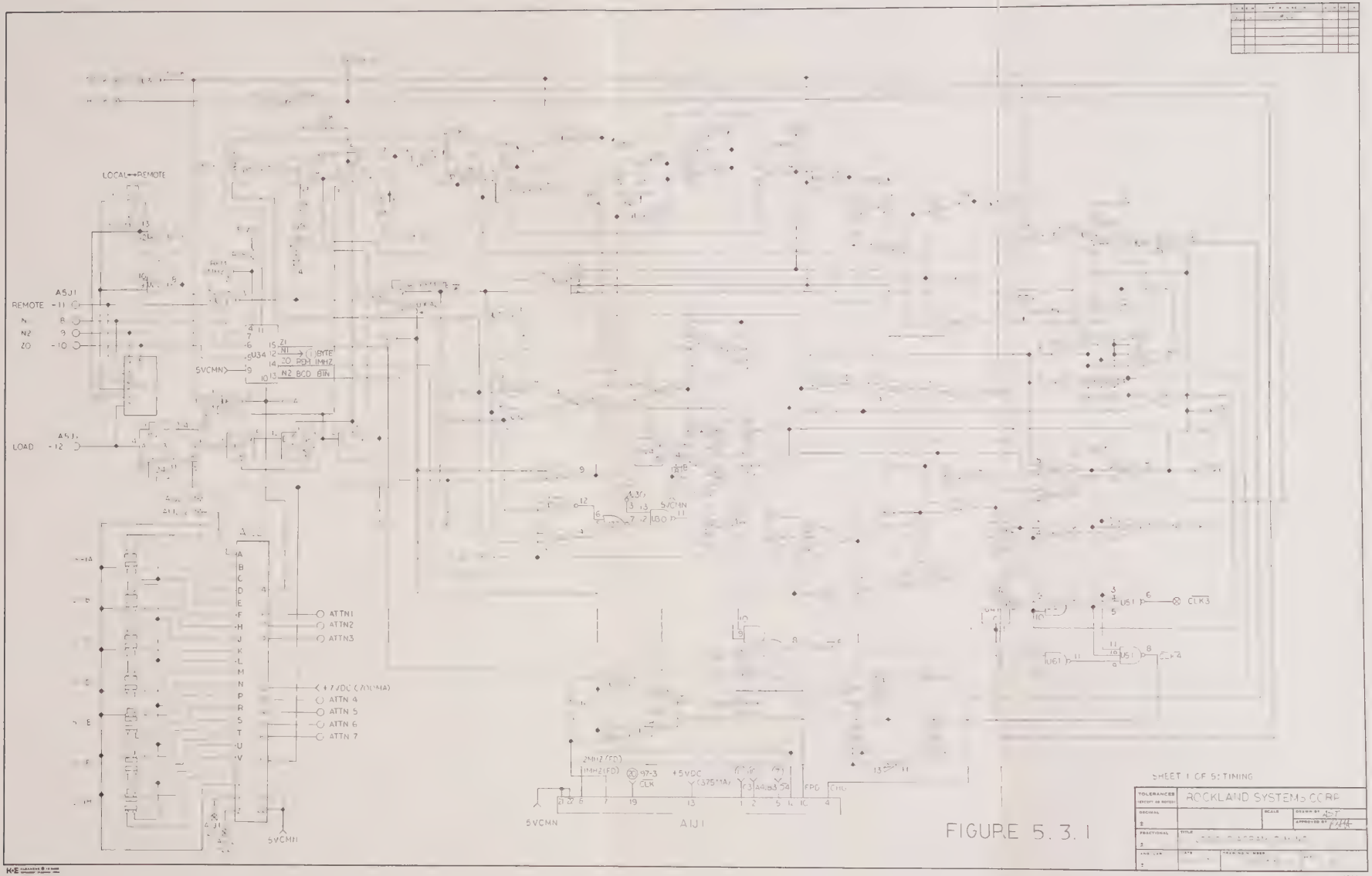
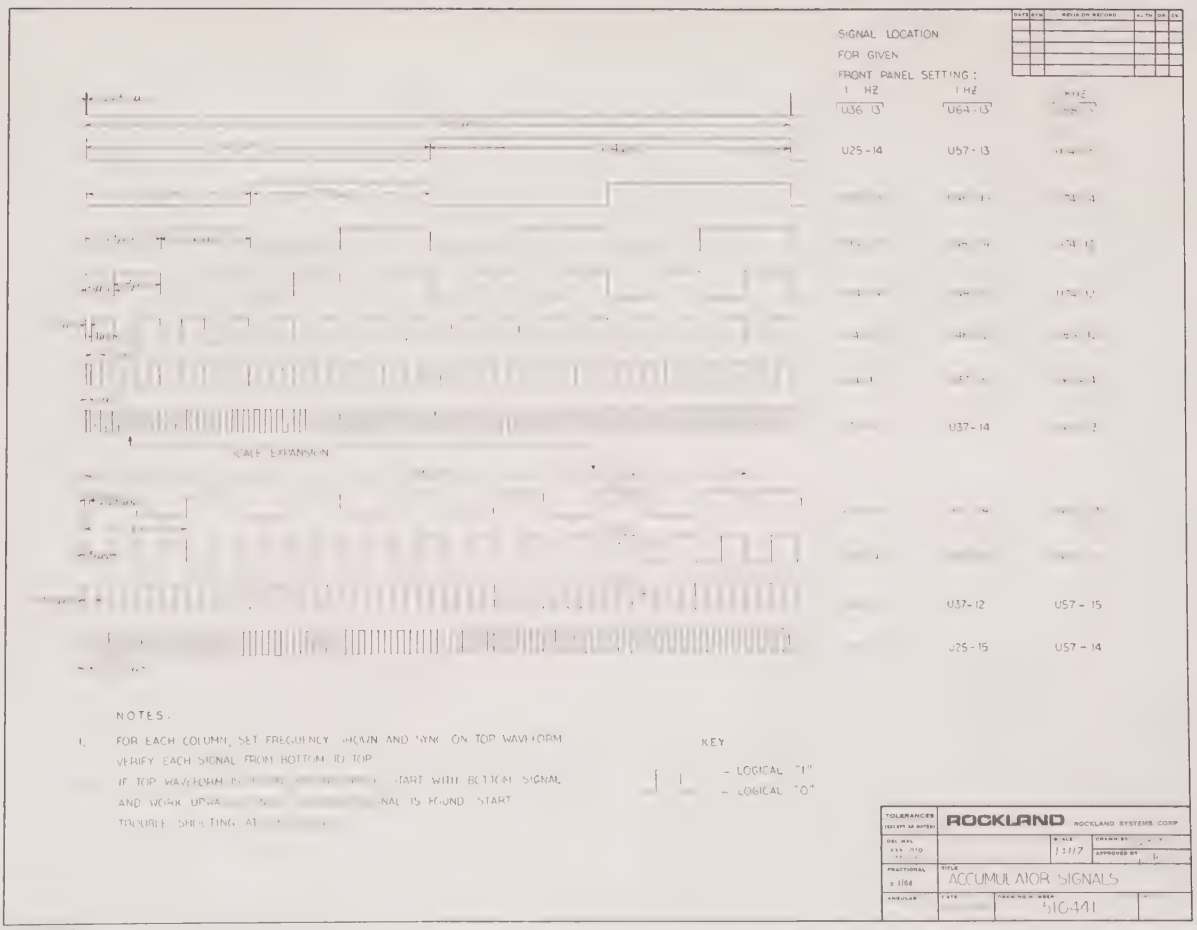
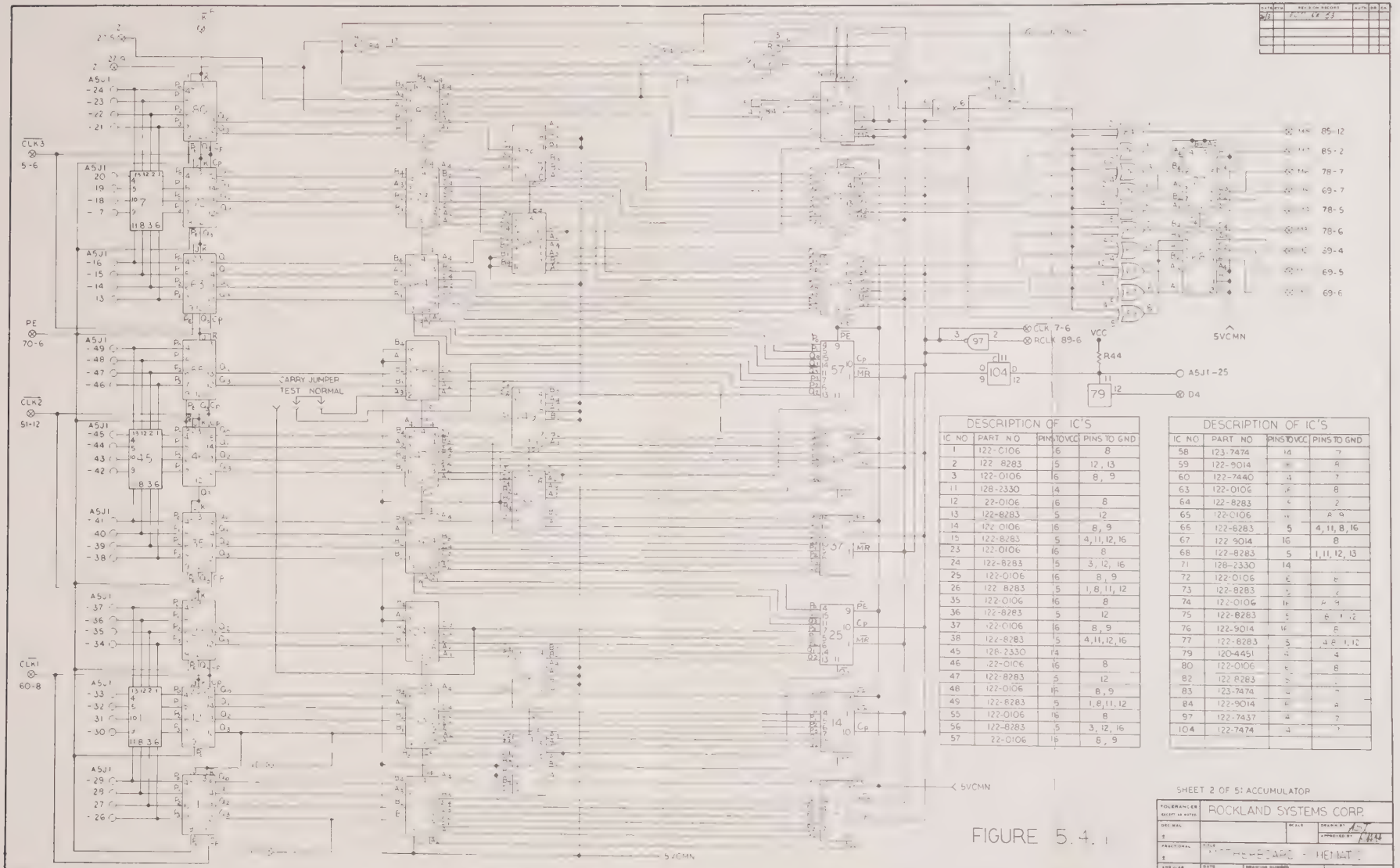

LOCAL↔REMOTE
A5J1
REMOTE - 11
N - 8
N2 - 9
Z0 - 10
LOAD - 12
A11J1
5VCMN
ATTN1
ATTN2
ATTN3
+7VDC (A1J1-A1A)
ATTN 4
ATTN 5
ATTN 6
ATTN 7
5VCMN1
2MHZ (FD)
1MHZ (FD)
97-3
CLK
+5VDC
(375 MA)
FPD
CHG
5VCMN
A1J1
CLK3
U61
U51
SHEET 1 OF 5: TIMING
ROCKLAND SYSTEMS CORP
TOLERANCES
DECIMAL
FRACTIONAL
ANG
SCALE
DRAWN BY
APPROVED BY
TITLE
DATE

FIGURE 5.3.1


SIGNAL LOCATION
FOR GIVEN
FRONT PANEL SETTING :
1 HZ
1 HZ
U36-13
U64-13
U25-14
U57-13
U37-14
SCALE EXPANSION
U37-12
U57-15
U25-15
U57-14
NOTES.
1. FOR EACH COLUMN, SET FREQUENCY SHOWN AND SYNC ON TOP WAVEFORM
VERIFY EACH SIGNAL FROM BOTTOM TO TOP
IF TOP WAVEFORM IS START WITH BOTTOM SIGNAL
AND WORK UPWA NAL IS FOUND START
TROUBLE SHOOTING AT
KEY
- LOGICAL "1"
- LOGICAL "0"
DATE BY
REVISION RECORD
ROCKLAND
ROCKLAND SYSTEMS CORP
TOLERANCES
DECIMAL
FRACTIONAL
± 1/64
ANGULAR
SCALE
1:1
DRAWN BY
APPROVED BY
TITLE
ACCUMULATOR SIGNALS
DATE
DRAWING NUMBER
510-441



DESCRIPTION OF IC'S			
IC NO	PART NO	PINS TO VCC	PINS TO GND
1	122-0106	16	8
2	122-8283	5	12, 13
3	122-0106	16	8, 9
11	128-2330	14	
12	22-0106	16	8
13	122-8283	5	12
14	122-0106	16	8, 9
15	122-8283	5	4, 11, 12, 16
23	122-0106	16	8
24	122-8283	5	3, 12, 16
25	122-0106	16	8, 9
26	122-8283	5	1, 8, 11, 12
35	122-0106	16	8
36	122-8283	5	12
37	122-0106	16	8, 9
38	122-8283	5	4, 11, 12, 16
45	128-2330	14	
46	22-0106	16	8
47	122-8283	5	12
48	122-0106	16	8, 9
49	122-8283	5	1, 8, 11, 12
55	122-0106	16	8
56	122-8283	5	3, 12, 16
57	22-0106	16	8, 9

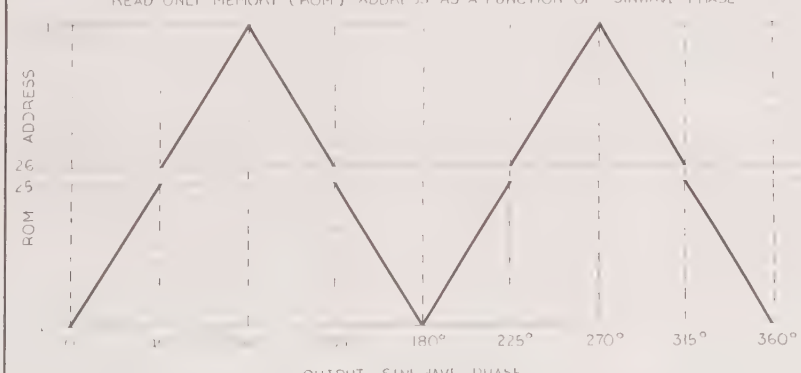
DESCRIPTION OF IC'S			
IC NO	PART NO	PINS TO VCC	PINS TO GND
58	123-7474	14	7
59	122-9014	16	8
60	122-7440	14	7
63	122-0106	16	8
64	122-8283	5	12
65	122-0106	16	8, 9
66	122-8283	5	4, 11, 8, 16
67	122-9014	16	8
68	122-8283	5	1, 11, 12, 13
71	128-2330	14	
72	122-0106	16	8
73	122-8283	5	12
74	122-0106	16	8, 9
75	122-8283	5	8, 11, 12
76	122-9014	16	8
77	122-8283	5	4, 8, 11, 12
79	120-4451	14	4
80	122-0106	16	8
82	122-8283	5	12
83	123-7474	14	7
84	122-9014	16	8
97	122-7437	14	7
104	122-7474	14	7

FIGURE 5.4.1

SHEET 2 OF 5: ACCUMULATOR

TOLERANCES EXCEPT AS NOTED	ROCKLAND SYSTEMS CORP.
DEC. MAC.	SCALE
FRACTIONAL	TITLE ARITHMETIC - HELMET
ANGULAR	DATE 1-20-72
	DRAWING NUMBER 510331-2 REV B

READ ONLY MEMORY (ROM) ADDRESS AS A FUNCTION OF SINWAVE PHASE



Address Bits	Location	Weight	Address Examples 38	144	265
ADR 0 (MSB)	U94-6	256	0	0	1
ADR 1	U94-5	128	0	1	0
ADR 2	U94-4	64	0	0	0
ADR 3	U94-3	32	1	0	0
ADR 4	U94-2	16	0	1	0
ADR 5	U94-1	8	0	0	1
ADR 6	U94-23	4	1	0	0
ADR 7	U94-22	2	1	0	0
ADR 8 (LSB)	U94-21	1	0	0	1

Logical "1" = 2.0 to 5.0 Volts

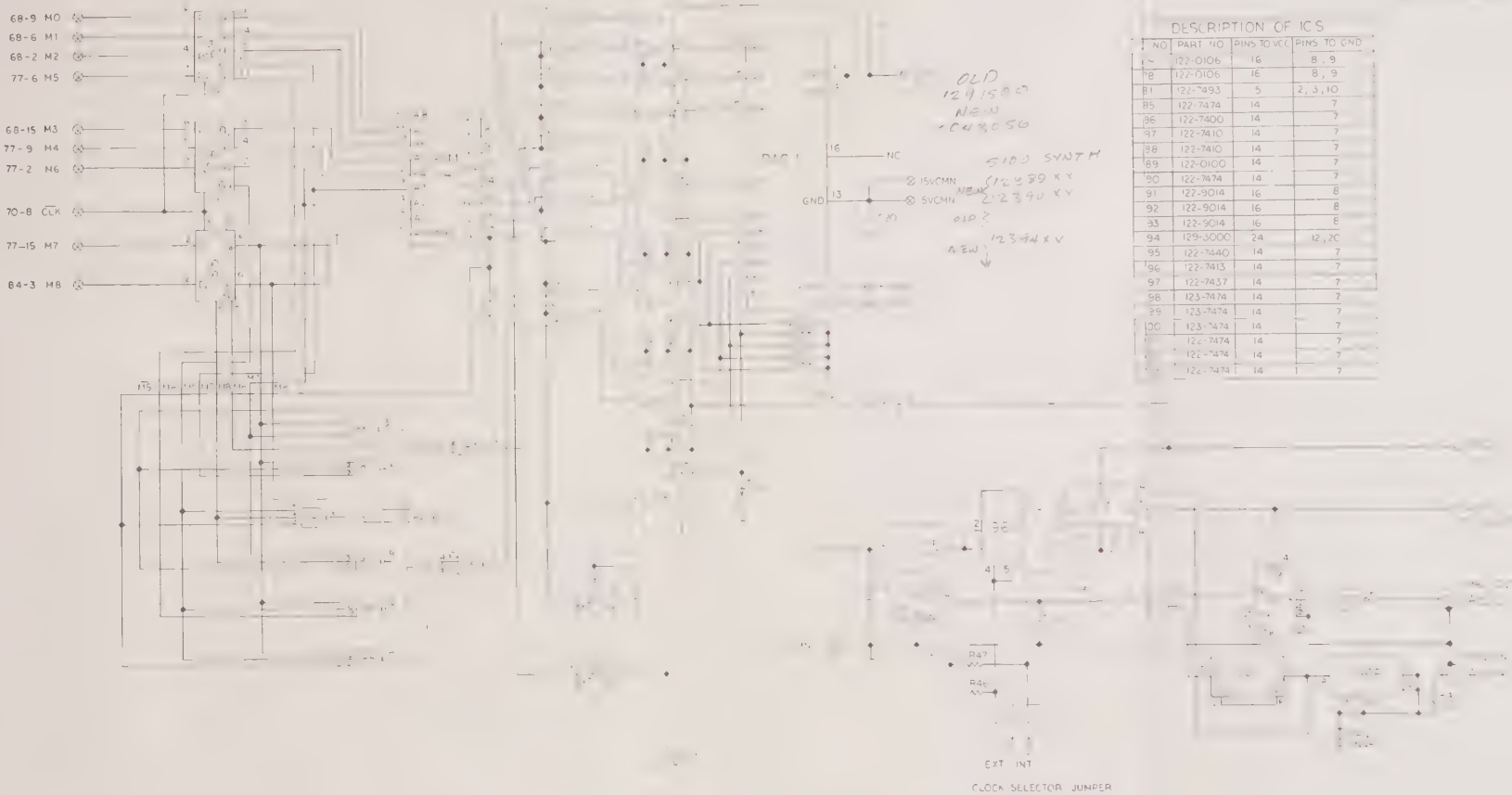
Logical "0" = 0.0 to 0.8 Volts

NOTES

1. ROM IS ARRANGED IN 512 X 8 STRUCTURE. 500 WORDS ARE USED TO STORE RELATIVE MAGNITUDE OF SINE FUNCTION FROM 0° TO 90°. ADDRESSES 6 THROUGH 255 STORE 0° TO 45° AND ADDRESSES 262 THROUGH 511 STORE 45° THROUGH 90°.
2. ABOVE GRAPH SHOWS HOW ROM IS ADDRESSED TO PRODUCE 360° SINEWAVE. INVERSION AFTER ROM PROVIDES NEGATIVE OPERATION FOR 180° TO 360°.
3. WITH FRONT PANEL SETTING OF 4 KHZ ADDRESS IS INCREMENTED ONE STEP PER 125 NSEC = SAMPLING RATE. EACH ADDRESS STEP CORRESPONDS TO A PHASE STEP OF 0.18°. DURING ONE SINE CYCLE THERE ARE 2,000 SAMPLES. (2,000 X 0.18° = 360°)
4. EACH OF THE NINE ADDRESS BITS MAY BE MONITORED AND VERIFIED BY DISPLAYING DAC-1 ON SCOPE. SEE SECTION 3.3 AND FIGURE 3.3. DAC-1 HAS POSITIVE EDGE AT 0° PHASE OF THE OUTPUT SINEWAVE AND NEGATIVE EDGE AT 180°.
5. NON-CONFORMING ADDRESS BITS MAY BE DUE TO DEFECTIVE U69, U78, U85. OTHERWISE CHECK ACCUMULATOR MALFUNCTION.
6. SIGNALS DAC-4 THROUGH DAC-11 ARE GENERATED DIRECTLY FROM THE EIGHT OUTPUT BITS OF THE ROM. DAC-2 AND DAC-3 ARE SYNTHESIZED FROM DAC-4 AND ADR 8 THROUGH ADR 5. DAC-1 IS DERIVED DIRECTLY FROM THE ACCUMULATOR.

FIGURE 5.5

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP		
DECIMAL XXX .010 XX .02		SCALE	DRAWN BY AST
			APPROVED BY
FRACTIONAL ± 1/64	TITLE ROM ADDRESS SIGNALS		
ANGULAR ±	DATE 11-17-72	DRAWING NUMBER 510408	



DESCRIPTION OF ICS

NO	PART NO	PINS TO VCC	PINS TO GND
[illegible]	122-0106	16	8, 9
78	122-0106	16	8, 9
B1	122-7493	5	2, 3, 10
B5	122-7474	14	7
B6	122-7400	14	7
B7	122-7410	14	7
B8	122-7410	14	7
B9	122-0100	14	7
90	122-7474	14	7
91	122-9014	16	8
92	122-9014	16	8
93	122-9014	16	8
94	129-3000	24	12, 20
95	122-7440	14	7
96	122-7413	14	7
97	122-7437	14	7
98	123-7474	14	7
99	123-7474	14	7
100	123-7474	14	7
[illegible]	122-7474	14	7
[illegible]	122-7474	14	7
[illegible]	122-7474	14	7

NOTES.

[illegible] 23 ON OPTION-01 UNITS

FIGURE 5.5.1

SHEET 3 OF 5 CRYSTAL D/A

TOLERANCES UNLESS OTHERWISE SPECIFIED	ROCKLAND SYSTEM	
DECIMAL ±	SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE MOTHERBOARD SCHEMATIC	
ANGULAR ±	DATE 1-21-72	DRAWING NUMBER 510331-3 REV E

Figure 5.6 Motherboard Integrated Circuits Parts List

Designation	Description	Rockland Part Number
U1	U: 4 bit shift register	122-0106
U2	U: 4 bit full adder	122-8283
U3	U: 4 bit shift register	122-0106
U4	U: triple 3 in NAND gate	122-7410
U5	U: 4 bit shift register	122-0106
U6	U: hex inverter	122-7404
U7	U: quad NOR gate	122-9015
U8	U: dual D type flip flop	122-7474
U9	U: quad NOR gate	122-9015
U10	U: dual D type flip flop	122-7474
U11	U: Pull up net 3.3K 2% x 13	128-2330
U12	U: 4 bit shift register	122-0106
U13	U: 4 bit full adder	122-8283
U14	U: 4 bit shift register	122-0106
U15	U: 4 bit full adder	122-8283
U16	U: quad 2 in NAND gate	122-7400
U17	U: dual D type flip flop	122-7474
U18	U: quad 2 in NAND gate	122-7400
U19	U: dual 4 in NAND buffer	122-7440
U20	U: dual D type flip flop	122-7474
U21	U: Pull up net 3.3K 2% x 13	128-2330
U22	U: quad 2 in NAND gate	122-7400
U23	U: 4 bit shift register	122-0106
U24	U: 4 bit full adder	122-8283
U25	U: 4 bit shift register	122-0106
U26	U: 4 bit full adder	122-8283
U27	U: dual D type flip flop	122-7474
U28	U: quad 2 in NAND gate	122-7400
U29	U: dual D type flip flop	122-7474
U30	U: quad 2 in NAND gate	122-7400
U31	U: monostable multivibrator	122-0100
U32	U: quad NOR gate	122-9015
U33	U: quad NOR gate	122-9015
U34	U: 4 bit shift register	122-0106
U35	U: 4 bit shift register	122-0106
U36	U: 4 bit full adder	122-8283
U37	U: 4 bit shift register	122-0106
U38	U: 4 bit full adder	122-8283
U39	U: dual 2 in 2 w AOI gate	122-7451
U40	U: quad 2 in NAND gate	122-7400
U41	U: dual D type flip flop	122-7474
U42	U: dual D type flip flop	122-7474
U43	U: 4 bit full adder	122-8283

Figure 5.6 Motherboard Integrated Circuits Parts List

Designation	Description	Rockland Part Number
U44	U: dual D type flip flop	122-7474
U45	U: pull up net 3.3K 2% x 13	128-2330
U46	U: 4 bit shift register	122-0106
U47	U: 4 bit full adder	122-8283
U48	U: 4 bit shift register	122-0106
U49	U: 4 bit full adder	122-8283
U50	U: hex inverter	122-7404
U51	U: triple 3 in NAND gate	122-7410
U52	U: triple 3 in NAND gate	122-7410
U53	U: 4 bit shift register	122-0106
U54	U: dual D type flip flop	122-7474
U55	U: 4 bit shift register	122-0106
U56	U: 4 bit full adder	122-8283
U57	U: 4 bit shift register	122-0106
U58	U: dual D type flip flop	123-7474
U59	U: quad XOR gate, inverted output	122-9014
U60	U: dual 4 in NAND buffer	122-7440
U61	U: quad 2 in NAND gate	122-7400
U62	U: triple 3 in NAND gate	122-7410
U63	U: 4 bit shift register	122-0106
U64	U: 4 bit full adder	122-8283
U65	U: 4 bit shift register	122-0106
U66	U: 4 bit full adder	122-8283
U67	U: quad XOR gate inverted output	122-9014
U68	U: 4 bit full adder	122-8283
U69	U: 4 bit shift register	122-0106
U70	U: quad 2 in NAND buffer	122-7437
U71	U: Pull up net 3.3K 2% x 13	128-2330
U72	U: 4 bit shift register	122-0106
U73	U: 4 bit full adder	122-8283
U74	U: 4 bit shift register	122-0106
U75	U: 4 bit full adder	122-8283
U76	U: quad XOR gate inverted output	122-9014
U77	U: 4 bit full adder	122-8283
U78	U: 4 bit shift register	122-0106
U79	U: dual peripheral driver	122-4451
U80	U: 4 bit shift register	122-0106
U81	U: 4 bit counter	122-7493
U82	U: 4 bit full adder	122-8283
U83	U: dual D type flip flop	123-7474
U84	U: quad XOR gate inverted output	122-9014
U85	U: dual D type flip flop	122-7474

Figure 5.6 Motherboard Integrated Circuits Parts List

Designation	Description	Rockland Part Number
U86	U: quad 2 in NAND gate	122-7400
U87	U: triple 3 in NAND gate	122-7410
U88	U: triple 3 in NAND gate	122-7410
U89	U: monostable multivibrator	122-0100
U90	U: dual D type flip flop	122-7474
U91	U: quad XOR gate inverted output	122-9014
U92	U: quad XOR gate inverted output	122-9014
U93	U: quad XOR gate inverted output	122-9014
U94	U: ROM 512 x 8	129-3000
U95	U: dual 4 in NAND buffer	122-7440
U96	U: dual NAND Schmitt trigger	122-7413
U97	U: quad 2 in NAND buffer	122-7437
U98	U: dual D type flip flop	123-7474
U99	U: dual D type flip flop	123-7474
U100	U: dual D type flip flop	123-7474
U101	U: dual D type flip flop	122-7474
U102	U: dual D type flip flop	122-7474
U103	U: dual D type flip flop	122-7474
U104	U: dual D type flip flop	122-7474
R2	R: fxd metflm 2.00 K 1% 1/8 W	111-2000
R3	R: fxd comp 10 K 5% 1/4W	116-3101
R4	R: fxd comp 100 ohm 5% 1/4 W	116-1101
R44	R: fxd comp 1 K 5% 1/4 W	116-2101
R46	R: fxd comp 3.3 K 5% 1/4 W	116-2331
R47	R: fxd comp 3.3 K 5% 1/4 W	116-2331
R50	R: fxd comp 220 ohm 5% 1/4 W	116-1221
R51	R: fxd comp 220 ohm 5% 1/4 W	116-1221
R52	R: fxd comp 220 ohm 5% 1/4 W	116-1221
R53*	R: fxd comp 220 ohm 5% 1/4 W	116-1221
R54*	R: fxd comp 220 ohm 5% 1/4 W	116-1221
R55	R: fxd comp 3.3 K 5% 1/4 W	116-2331
C	C: fxd cer 0.1 uf + 80 - 20% 10 V	100-4100
C12	C: fxd mica dipped 22 pf 10% 500 V	101-0220
C13	C: fxd tant 10 uf 20% 25 V	109-6100
C17	C: var mica 24 - 200 pf 175 V	108-1200
C24	C: fxd mica dipped 150 pf 10% 500 V	101-1150
CR4	CR: sil low leak 70 PIV 200 mW	132-0457

* NOT required on most units

Figure 5.6.1 Integrated Circuit Manufacturers Cross Reference List

Rockland Part No.	Texas Inst.	Fairchild	National	Signetics
122-0100	SN74121N	74121 DC	DM74121N	N74121A
122-0102	SN74166N			N74166B
122-0106	SN74195N			
122-4451	SN75451P		LM75451A	
122-7400	SN7400N	7400 DC	DM7400N	N7400A
122-7404	SN7404N	7404 DC	DM7404N	N7404A
122-7410	SN7410N	7410 DC	DM7410N	N7410A
122-7413	SN7413N	7413 DC	DM7413N	N7413A
122-7437	SN7437N	7437 DC	DM7437N	N7437A
122-7440	SN7440N	7440 DC	DM7440N	N7440A
122-7451	SN7451N	7451 DC	DM7451N	N7451A
122-7474	SN7474N	7474 DC	DM7474N	N7474A
122-7493	SN7493N	7493 DC	DM7493N	N7493A
122-8283			DM8283N	N7483B
122-9014		9014 DC		
122-9015		9015 DC		
122-9328		9328 DC		
123-7474	SN74H74N	74H74 DC	DM74H74N	N74H74A
128-2330	Beckman No. 899-1-R3.3K			
129-3000	Custom Programmed ROM - Available only from Rockland Systems Corporation			

Figure 5.7 Output Amplifier Parts List

Designation	Description	Rockland Part Number
C26	C: fxd mica 51 pf ±10% 500 WVDC	101-0510
C27	C: fxd tant elect 10.0 MFD ±20% 25 WVDC	109-6100
C28	C: fxd mylar 0.01 MFD ±10% 100 WVDC	105-3100
C29	C: fxd elect 50 MFD 25 WVDC	109-6500
C30	C: fxd mylar 0.01 MFD ±10% 100 WVDC	105-3100
C31	C: fxd elect 50 MFD 25 WVDC	109-6500
C32	C: fxd mica 1000 pf ±1% 500 WVDC	101-2101
C33	C: fxd mica 1100 pf ±1% 500 WVDC	101-2111
CR10	Diode: sil zener 20 V ±5% 400 MW	131-0200
CR11	Diode: sil gen purp 70 PIV	132-0457
CR12	Diode: sil gen purp 70 PIV	132-0457
CR13	Diode: sil gen purp 70 PIV	132-0457
L1	Inductor: fxd 6.8 UHY ±10%	168-5000
LPF-1	Filter: low pass DC-2 MHZ ±.25db	165-3000
Q8 & Q9	Transistor: silicon NPN matched pair	134-0065
Q10	Transistor: silicon NPN	134-3568
Q13	Transistor: silicon NPN	134-3568
Q14	Transistor: silicon PNP	136-4354
Q15	Transistor: silicon NPN	134-3568
Q16	Transistor: silicon PNP	136-4354
A4R1	R: var comp 1K ±10% 1/2 W	118-2107
R19	R: var cermet 5K ±10% 3/4 W	118-2500
R20	R: fxd comp 27K ±5% 1/4 W	116-3271
R22	R: fxd comp 620 ohm ±5% 1/4 W	116-1621
R23	R: fxd comp 220 ohm ±5% 1/4 W	116-1221
R25	R: fxd comp 820 ohm ±5% 1/4 W	116-1821
R26	R: fxd comp 100 ohm ±5% 1/4 W	116-1101
R27	R: fxd comp 2.2K ±5% 1/4 W	116-2221
R28	R: fxd comp 2.2K ±5% 1/4 W	116-2221
R29	R: var cermet 5K ±10% 3/4 W	118-2500
R30	R: fxd met film 1K ±1% 1/8 W	111-1000
R31	R: fxd comp 560 ohm ±5% 1/4 W	116-1561
R32	R: fxd met film 15K ±1% 1/8 W	112-1500
R33	R: fxd comp 2.2K ±5% 1/4 W	116-2221
R34	R: fxd comp 47 ohm ±5% 1/4 W	116-0471
R35	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
R36	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
R38	R: fxd comp 10K ±5% 1/4 W	116-3101
R39	R: fxd comp 1K ±5% 1/4 W	116-2101
R40	R: fxd met film 49.9 ohm ±1% 1/8 W	119-4990
R41	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
R42	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
R43	R: fxd comp 560 ohm ±5% 1/4 W	116-1561

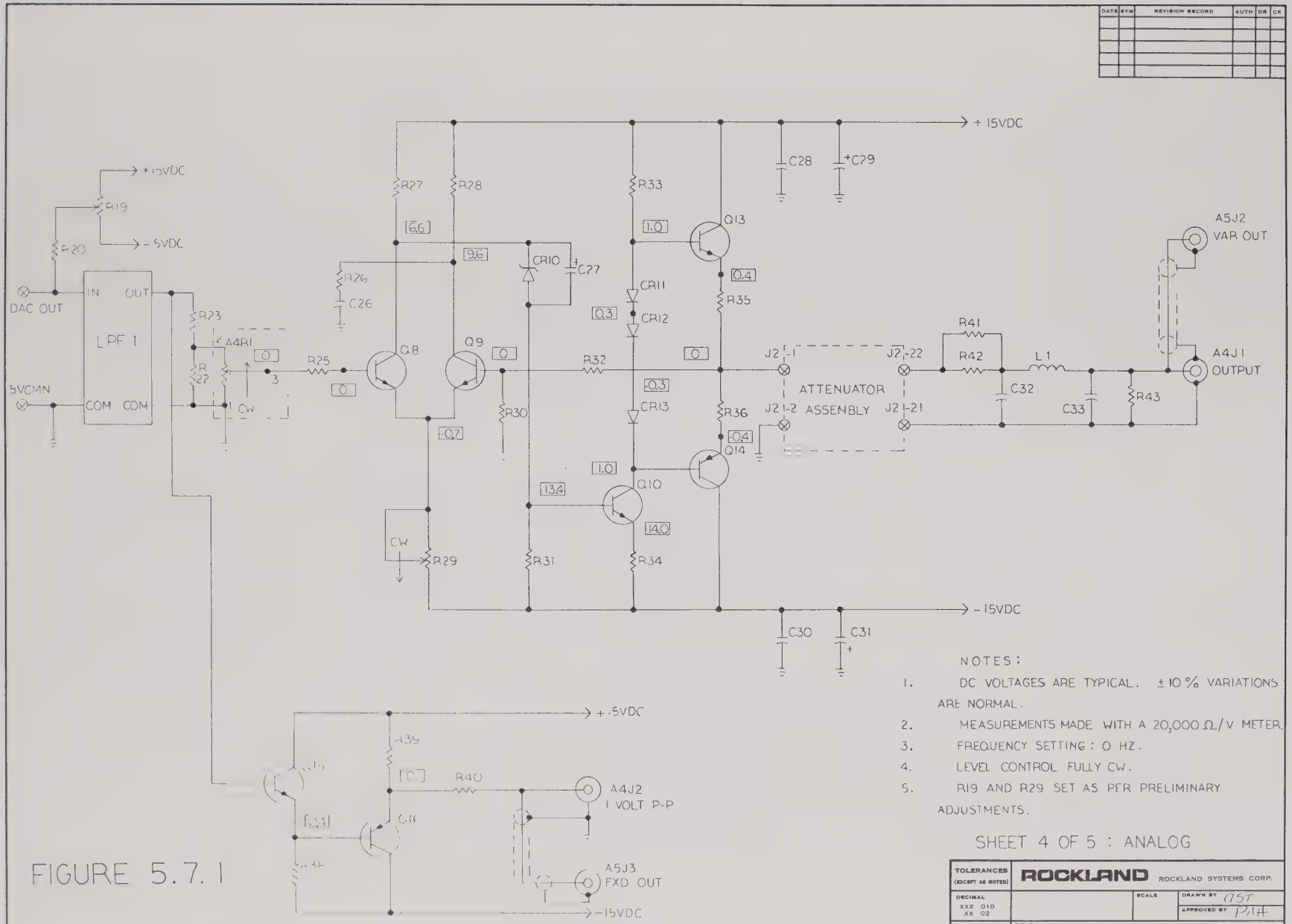


FIGURE 5.7.1

NOTES:

1. DC VOLTAGES ARE TYPICAL. ±10% VARIATIONS ARE NORMAL.
2. MEASUREMENTS MADE WITH A 20,000 Ω/V METER.
3. FREQUENCY SETTING: 0 HZ.
4. LEVEL CONTROL FULLY CW.
5. R19 AND R29 SET AS PER PRELIMINARY ADJUSTMENTS.

SHEET 4 OF 5 : ANALOG

REVISION RECORD					
DATE	BY/M		AUTH	DR	CK

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP.		
DECIMAL XXX .010 XX .02		SCALE	DRAWN BY RST
			APPROVED BY PJH
FRACTIONAL ± 1/64	TITLE MOTHERBOARD SCEMATIC		
ANGULAR ±	DATE 11-11-71	DRAWING NUMBER 510331-4	REV B

Figure 5.8 Power Supply Parts List

Designation	Description	Rockland Part Number
A5CR1	Diode: Silicon, FWB, 50PIV, 12A	130-0540
A5T1	Transformer: Power	177-3005
A5B1	Fan: 115V, 15W	165-0701
A5F1	Fuse: 3AG 1A SB	165-4002
A5S1	Switch: Slide DPDT	342-2201
A5C1	C: Fxd Ceramic .01 MFD, 1,000V	100-3100
A5C2	C: Fxd Ceramic .01 MFD, 1,000V	100-3100
A4S3	Switch: Push Button, Line	341-3100
CR2	Rectifier: Silicon, FWB, 200PIV, 1A	130-0541
CR3	Rectifier: Silicon, FWB, 200PIV, 1A	130-0541
CR5	Rectifier: Silicon, 200PIV, 1A	130-2110
C1	C: Fxd, Elect, 10,000 MFD, 15WVDC	109-9100
C2	C: Fxd, Elect, 10,000 MFD, 15WVDC	109-9100
C3	C: Fxd, Elect, 10,000 MFD, 15WVDC	109-9100
C4	C: Fxd, Tant. Elect, 0.1 MFD ±20%, 35WVDC	109-4100
C5	C: Fxd, Tant. Elect, 0.1 MFD ±20%, 35WVDC	109-4100
C6	C: Fxd, Elect, 3,000 MFD, 50WVDC	109-8300
C7	C: Fxd, Elect, 3,000 MFD, 50WVDC	109-8300
C8	C: Fxd, Tant. Elect, 0.1 MFD, ±20%, 35WVDC	109-4100
C10	C: Fxd, Tant. Elect, 0.1 MFD, ±20%, 35WVDC	109-4100
C50	C: Fxd, Tant. Elect, 0.1 MFD, ±20%, 35WVDC	109-4100
C51	C: Fxd, Tant. Elect, 0.1 MFD, ±20%, 35WVDC	109-4100
Q1	Regulator: Voltage, 5V ±10%	120-0050
Q2	Regulator: Voltage, 5V ±10%	120-0050
Q3	Regulator: Voltage, 5V ±10%	120-0050
Q4	Regulator: Voltage, 15V ±10%	120-0151
Q5	Regulator: Voltage, 15V ±10%	120-0151

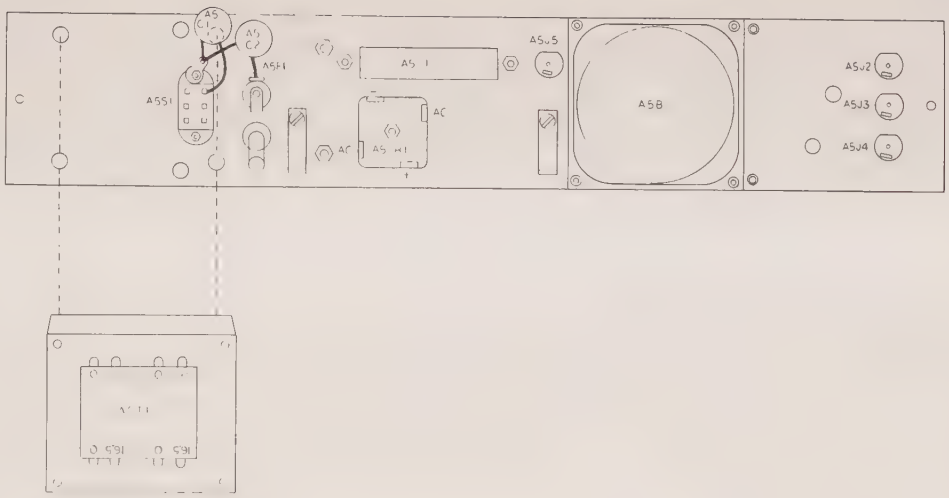
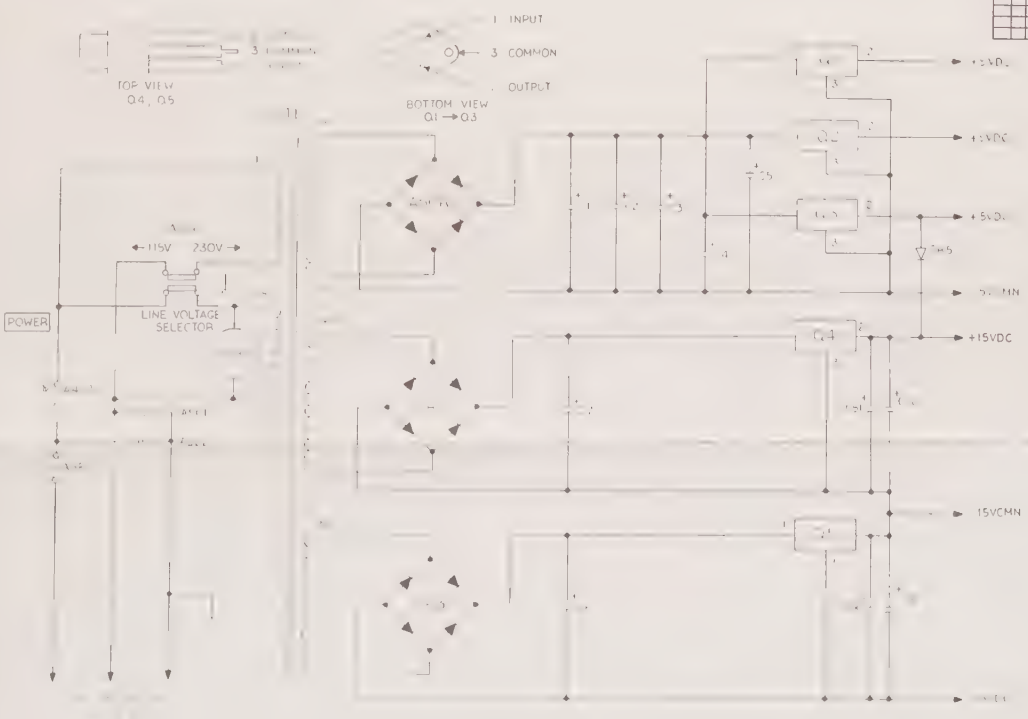


FIGURE 5.8.1 REAR PANEL ASSEMBLY

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP	
DECIMAL .XX ±.010 .XXX ±.002	SCALE 1 : 1	DRAWN BY T.S.T. APPROVED BY R.M.H.
FRACTIONAL ± 1/64	TITLE REAR PANEL ASSEMBLY - A5	
ANGULAR ±	DATE 10-25-72	DRAWING NUMBER 510404 REV A



SHEET 5 OF 5: POWER

ABBREVIATED FOR A5S1 A1

FIGURE 5.8.2

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND	
DECIMAL	SCALE	DRAWN BY APPROVED BY
FRACTIONAL	TITLE	
ANGULAR	DATE	DRAWING NUMBER 510331-5 REV

Figure 5.9 Standard Attenuator Parts List

Designation	Description	Rockland Part Number
R1	R: Fxd, Met.Flm, 49.9OHM ±1%, 1/8W	119-4990
R2	R: Fxd, Met.Flm, 887OHM ±1%, 1/8W	110-8870
R3	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R4	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R5	R: Fxd, Met. Flm, 887 OHM, ±1%, 1/8W	110-8870
R6	R: Fxd, Met. Flm, 432 OHM, ±1%, 1/8W	110-4320
R7	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R8	R: Fxd, Met. Flm, 432 OHM, ±1%, 1/8W	110-4320
R9	R: Fxd, Met. Flm, 221 OHM, ±1%, 1/8W	110-2210
R10	R: Fxd, Met. Flm, 23.7 OHM, ±1%, 1/8W	119-2370
R11	R: Fxd, Met. Flm, 221 OHM, ±1%, 1/8W	110-2210
R12	R: Fxd, Met. Flm, 115 OHM, ±1%, 1/8W	110-1150
R13	R: Fxd, Met. Flm, 51.1 OHM, ±1%, 1/8W	119-5110
R14	R: Fxd, Met. Flm, 115 OHM, ±1%, 1/8W	110-1150
R15	R: Fxd, Met. Flm, 97.6 OHM,±1%, 1/8W	119-9760
R16	R: Fxd, Met. Flm, 71.5 OHM,±1%, 1/8W	119-7150
R17	R: Fxd, Met. Flm, 97.6 OHM,±1%, 1/8W	119-9760
R18	R: Fxd, Met. Flm, 61.9 OHM,±1%, 1/8W	119-6190
R19	R: Fxd, Met. Flm, 249 OHM,±1%, 1/8W	110-2490
R20	R: Fxd, Met. Flm, 61.9 OHM,±1%, 1/8W	119-6190
R21	R: Fxd, Met. Flm, 51.1 OHM,±1%, 1/8W	111-5110
R22	R: Fxd, Met. Flm, 2.61K OHM,±1%, 1/8W	111-2610
R23	R: Fxd, Met. Flm, 51.1 K OHM, ±1%, 1/8W	119-5110

DATE	BY	REVISION RECORD	AUTH	DR	CK

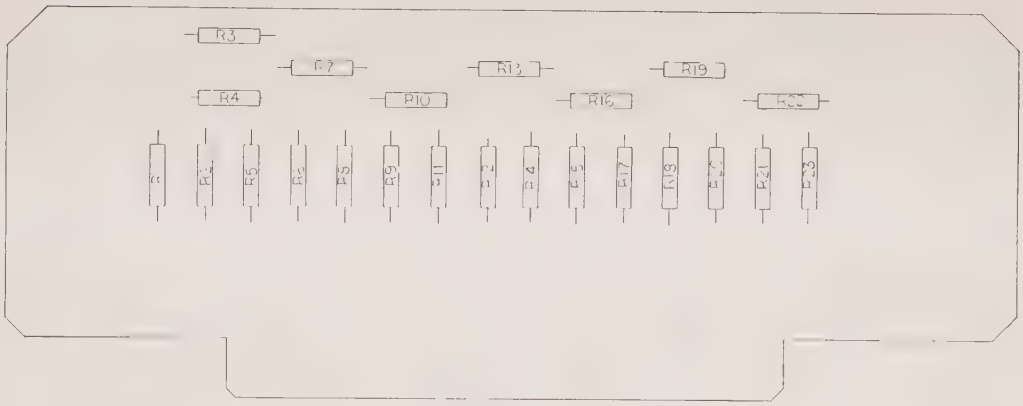


FIGURE 5.9.1

TOLERANCES (EXCEPT AS NOTED)	HICKLAND SYSTEMS CORP	
DECIMAL ±		SCALE / DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE: MANUAL ATTENUATOR ASSEMBLY	
ANGULAR ±	DATE: 10-15-71	DRAWING NUMBER: 10340 REV

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DATE	BY	REVISION RECORD	AUTH	DR	CK

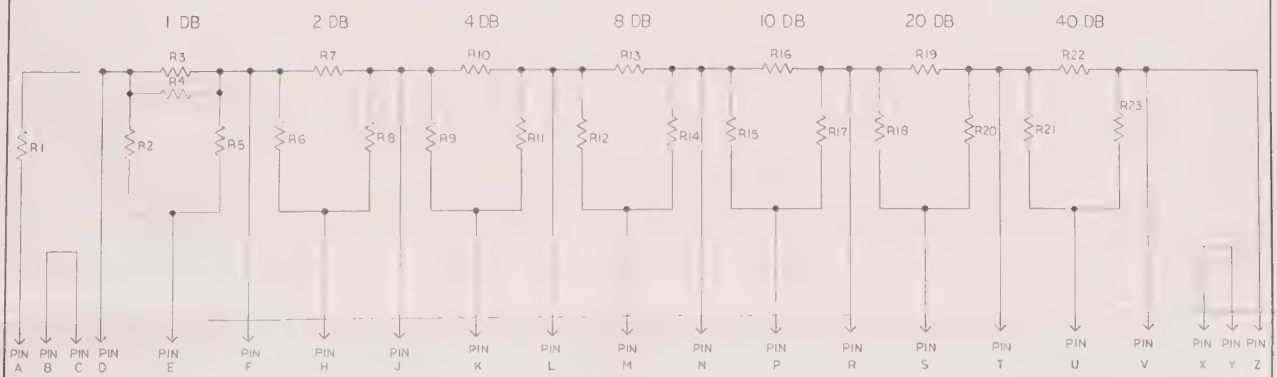

FIGURE 5.9.2

TOLERANCES (EXCEPT AS NOTED)		
DECIMAL ±		SCALE / DRAWN BY / APPROVED BY
FRACTIONAL ±	TITLE	
ANGULAR ±	DATE / DRAWING NUMBER	REV

Figure 5.10 Programmable Attenuator Parts List

Designation	Description	Rockland Part Number
C1	C: Fxd, Tant. Elect., 0.1 MFD ±20%, 35WVDC	109-4100
C2	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C3	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C4	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C5	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C6	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C7	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
K1	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K2	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K3	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K4	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K5	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K6	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K7	Relay: Crystal, DPDT, 5V, 160MW	175-1502
Q1	Regulator: Voltage, 5V ±10%	120-0050
R1	R: Fxd, Met.Flm, 49.9OHM ±1%, 1/8W	119-4990
R2	R: Fxd, Met.Flm, 887OHM ±1%, 1/8W	110-8870
R3	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R4	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R5	R: Fxd, Met. Flm, 887 OHM, ±1%, 1/8W	110-8870
R6	R: Fxd, Met. Flm, 432 OHM, ±1%, 1/8W	110-4320
R7	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R8	R: Fxd, Met. Flm, 432 OHM, ±1%, 1/8W	110-4320
R9	R: Fxd, Met. Flm, 221 OHM, ±1%, 1/8W	110-2210
R10	R: Fxd, Met. Flm, 23.7 OHM, ±1%, 1/8W	119-2370
R11	R: Fxd, Met. Flm, 221 OHM, ±1%, 1/8W	110-2210
R12	R: Fxd, Met. Flm, 115OHM, ±1%, 1/8W	110-1150
R13	R: Fxd, Met. Flm, 51.1 OHM, ±1%, 1/8W	119-5110
R14	R: Fxd, Met. Flm, 115OHM, ±1%, 1/8W	110-1150
R15	R: Fxd, Met. Flm, 97.6 OHM,±1%, 1/8W	119-9760
R16	R: Fxd, Met. Flm, 71.5 OHM,±1%, 1/8W	119-7150
R17	R: Fxd, Met. Flm, 97.6 OHM,±1%, 1/8W	119-9760
R18	R: Fxd, Met. Flm, 61.9 OHM,±1%, 1/8W	119-6190
R19	R: Fxd, Met. Flm, 249 OHM,±1%, 1/8W	110-2490
R20	R: Fxd, Met. Flm, 61.9 OHM,±1%, 1/8W	119-6190
R21	R: Fxd, Met. Flm, 51.1 OHM,±1%, 1/8W	111-5110
R22	R: Fxd, Met. Flm, 2.61K OHM,±1%, 1/8W	111-2610
R23	R: Fxd, Met. Flm, 51.1 K OHM, ±1%, 1/8W	119-5110
R24	R: Fxd, Comp., 1.0K OHM,±5%, 1/4W	116-2101
R25	R: Fxd, Comp., 2.2 K OHM, ±5%, 1/8W	116-2220
R26	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R27	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R28	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R29	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R30	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R31	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
U1	I.C.: Dual D-Type Flip-Flop	122-7474
U2	I.C.: Quad 2-In Nand Gate	122-7400
U3	I.C.: Dual D-Type Flip-Flop	122-7474
U4	I.C.: Quad 2-In Nand Gate	122-7400
U5	I.C.: Dual D-Type Flip-Flop	122-7474
U6	I.C.: Quad 2-In Nand Gate	122-7400
U7	I.C.: Dual D-Type Flip-Flop	122-7474
U8	I.C.: Quad 2-In Nand Gate	122-7400
U9	I.C.: Dual Peripheral Driver	120-4451
U10	I.C.: Dual Peripheral Driver	120-4451
U11	I.C.: Dual Peripheral Driver	120-4451
U12	I.C.: Dual Peripheral Driver	120-4451

DATE	SYM	REVISION RECORD	AUTH	DR	CK
2/3		ECO No 52			

COMPONENT SIDE

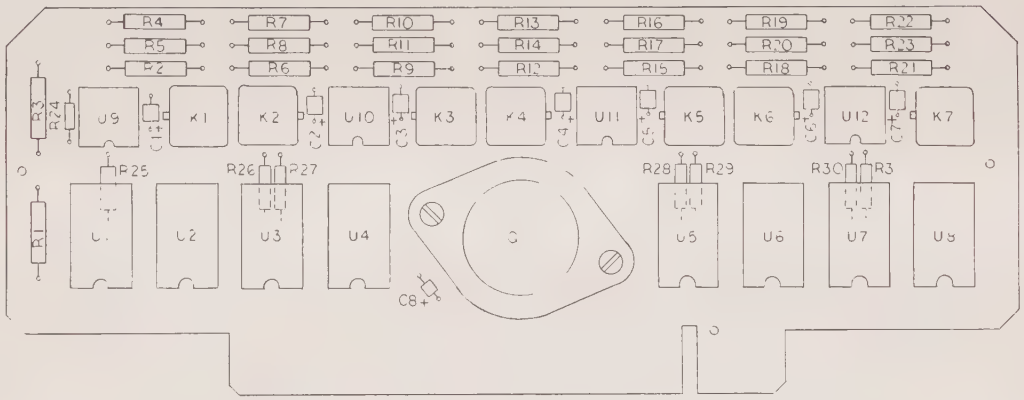

FIGURE 5.10.1

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND SYSTEMS CORP		
DECIMAL ±		SCALE	DRAWN BY AST
			APPROVED BY
FRACTIONAL ±	TITLE REMOTE ATTENUATOR ASSEMBLY		
ANGULAR ±	DATE 12-29-71	DRAWING NUMBER 510345	REV L

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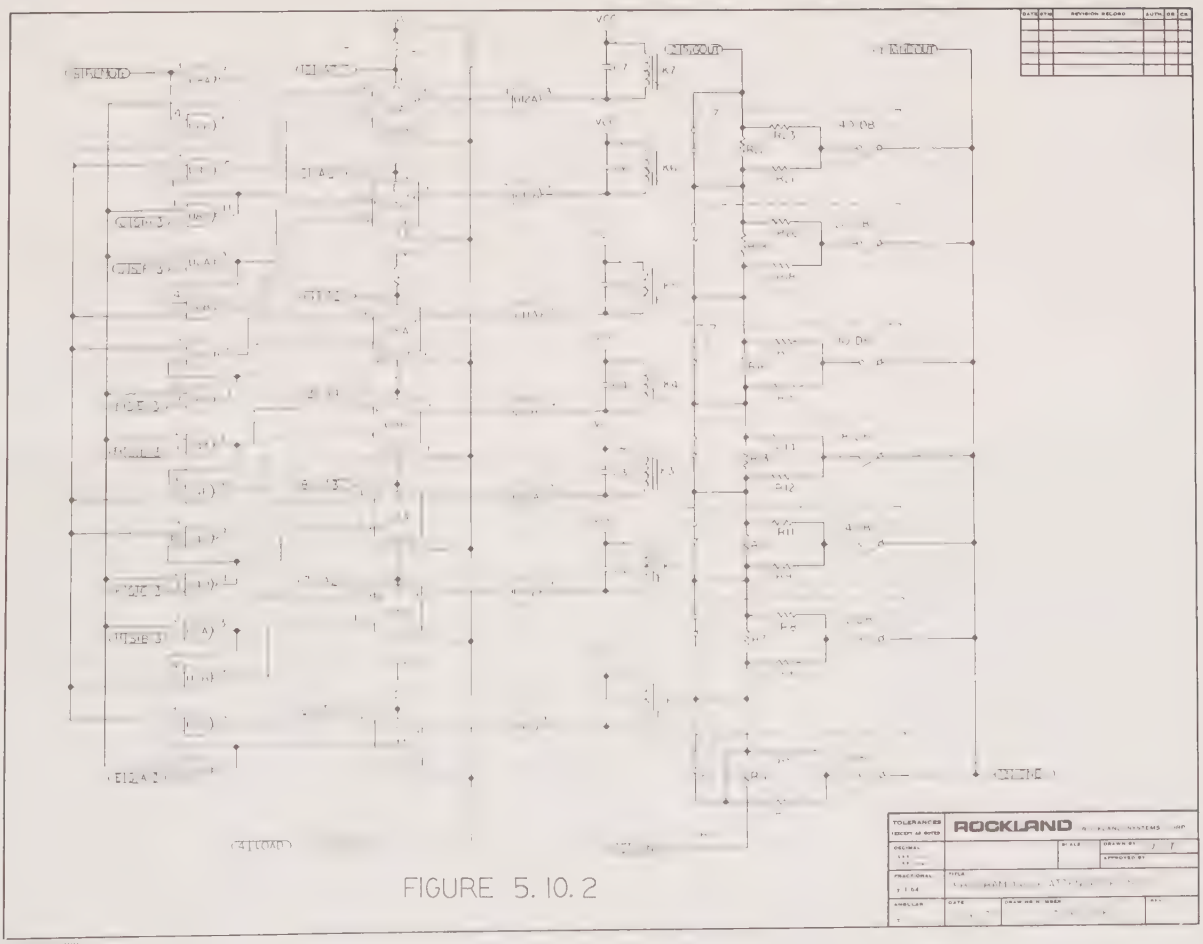
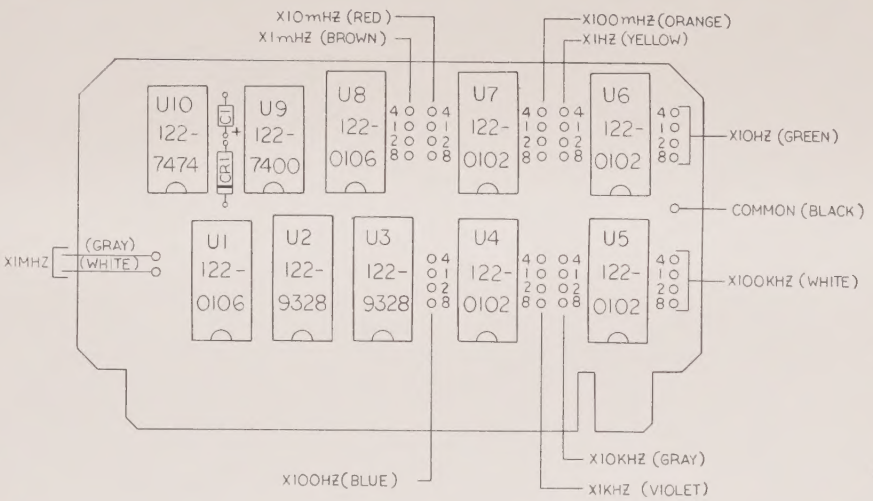
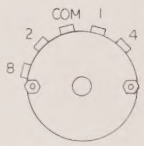


FIGURE 5.10.2

Figure 5.11 Front Panel Scanner Parts List

Designation	Description	Rockland Part Number
U1	U: 4 bit shift register	122-0106
U2	U dual 8 bit shift register	122-9328
U3	U· dual 8 bit shift register	122-9328
U4	U 8 bit shift register	122-0102
U5	U 8 bit shift register	122-0102
U6	U 8 bit shift register	122-0102
U7	U· 8 bit shift register	122-0102
U8	U 4 bit shift register	122-0106
U9	U quad 2 in NAND gate	122-7400
U10	U dual D type flip flop	122-7474
CR1	DIODE: Sil., Gen. Purp., 70 PIV	132-0457
C1	C: fixd. TANT. Elect., 68.0 MFD ± 20%, 6V	109-6680





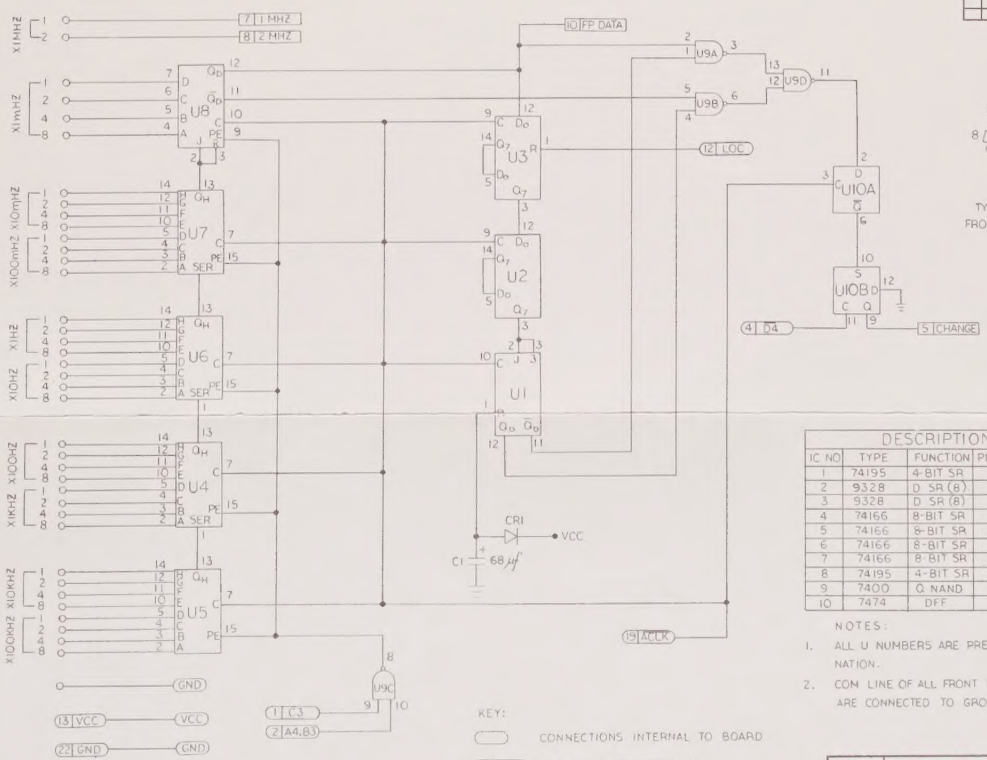
TYPICAL REAR VIEW
FRONT PANEL SWITCH

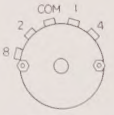
NOTES:

1. ALL U NUMBERS ARE PREFIXED WITH A2 DESIGNATION.
2. COM LINE OF FRONT PANEL SWITCHES ARE CONNECTED TO GRD.

FIGURE 5.11.1

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP.		
DECIMAL .XXX .010 .XX .02	ASSEMBLY A2	SCALE	DRAWN BY GST
			APPROVED BY
FRACTIONAL ± 1/64	TITLE FRONT PANEL SCANNER ASSEMBLY		
ANGULAR ±	DATE 9-1-72	DRAWING NUMBER 510435	REV





TYPICAL REAR VIEW
FRONT PANEL SWITCH

DESCRIPTION OF IC'S

IC NO	TYPE	FUNCTION	PINS TO VCC	PINS TO GND
1	74195	4-BIT SR	16	8
2	9328	D SR (8)	16	8, 7, 10
3	9328	D SR (8)	16	8, 7, 10
4	74166	8-BIT SR	16	8, 6
5	74166	8-BIT SR	16	8, 6
6	74166	8-BIT SR	16	8, 6
7	74166	8-BIT SR	16	8, 6
8	74195	4-BIT SR	16,1	8
9	7400	Q. NAND	14	7
10	7474	DFF	14	7, 12

NOTES:

1. ALL U NUMBERS ARE PREFIXED WITH A2 DESIGNATION.
2. COM LINE OF ALL FRONT PANEL SWITCHES ARE CONNECTED TO GROUND.

KEY:

CONNECTIONS INTERNAL TO BOARD

INPUT PIN CONNECTIONS

OUTPUT PIN CONNECTIONS

FIGURE 5.11.2

TOLERANCES (EXCEPT AS NOTED)	ROCKLAND ROCKLAND SYSTEMS CORP.		
DECIMAL .XXX .010 .XX .02	ASSEMBLY A2	SCALE	DRAWN BY GST
			APPROVED BY
FRACTIONAL ± 1/64	TITLE FRONT PANEL SCANNER		
ANGULAR ±	DATE 6-7-72	DRAWING NUMBER 510436	REV

ROCKLAND

MP MASTER
MA20102